The Tricon is designed with a fully triplicated architecture throughout, from the input modules through the main processors (MPs) to the output modules.

Theory of Operation

Fault tolerance in the Tricon is achieved by means of a Triple-Modular Redundant (TMR) architecture. The Tricon provides error-free, uninterrupted control in the presence of either hard failures of components, or transient faults from internal or external sources.

The Tricon is designed with a fully triplicated architecture throughout, from the input modules through the main processors to the output modules. Every I/O module houses the circuitry for three independent channels, which are also referred to as legs. Each channel on the input modules reads the process data and passes that information to its respective main processor. The three main processors communicate with each other using a proprietary high-speed bus system called the TriBus.

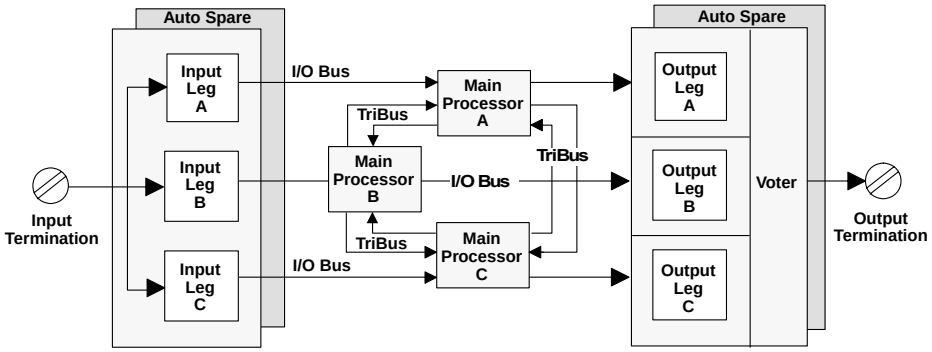
Once per scan, the three main processors synchronize and communicate with their two neighbors over the TriBus. The Tricon votes digital input data, compares output data, and sends copies of analog input data to each main processor.

The main processors execute the control program and send outputs generated by the control program to the output modules. The output data is voted on the output modules as close to the field as possible, which enables the Tricon to detect and compensate for any errors that might occur between the voting and the final output driven to the field.

For each I/O module, the system can support an optional hot-spare module which takes control if a fault is detected on the primary module during operation. The hot-spare position can also be used for online system repairs.

Main Processor Modules

A Tricon system contains three main processor (MP) modules to control three separate channels of the system. Each main processor operates in parallel with the other two main processors, as a member of a triad.



Simplified Tricon Architecture

A dedicated I/O and COMM processor on each main processor manages the data exchanged between the main processors and the I/O modules. A triplicated I/O bus is located on the chassis backplane and is extended from chassis to chassis by means of I/O bus cables.

As each input module is polled, the new input data is transmitted to the main processor over the appropriate channel of the I/O bus. The input data from each input module is assembled into a table in the main processor and stored in memory for use in the hardware voting process.

The individual input table in each main processor is transferred to its neighboring main processors over the proprietary TriBus. During this transfer, hardware voting takes place. The TriBus uses a direct memory access (DMA) programmable device to synchronize, transmit, vote and compare data among the three main processors.

If a disagreement is discovered, the signal value found in two out of three tables prevails, and the third table is corrected accordingly. One-time differences which result from sample timing variations can be distinguished from a pattern of differing data. The three independent main processors each maintain data about necessary corrections in local memory. Any disparity is flagged and used at the end of the scan by the built-in Fault Analyzer routines to determine whether a fault exists on a particular module.

After the TriBus transfer and input data voting have corrected the input values, these corrected values are used by the main processors as input to the user-written control program. (The control program is developed in the TriStation software and downloaded to the main processors.) The 32-bit main microprocessor executes the user-written control program in parallel with the neighboring main processor modules.

The user-written control program generates a table of output values based on the table of input values, according to the rules built into the control program by the customer. The I/O processor on each main processor manages the transmission of output data to the output modules by means of the I/O bus.

Using the table of output values, the I/O processor generates smaller tables, each corresponding to an individual output module in the system. Each small table is transmitted to the appropriate channel of the corresponding output module over the I/O bus. For example, Main Processor A transmits the appropriate table to Channel A of each output module over I/O Bus A. The transmittal of output data has priority over the routine scanning of all I/O modules.

The I/O and COMM processor manages the data exchanged between the main processors and the communication modules using the communication bus, which supports a broadcast mechanism.

The model 3008 Main Processors provide 16 megabytes of DRAM, which is used for the control program, sequence-of-events data, I/O data, diagnostics and communication buffers.

In the event of an external power failure, the integrity of the user-written program and the retentive variables is protected for a minimum of six months.

The main processor modules receive power from dual power modules and power rails in the main chassis. A failure on one power module or power rail will not affect the performance of the system.

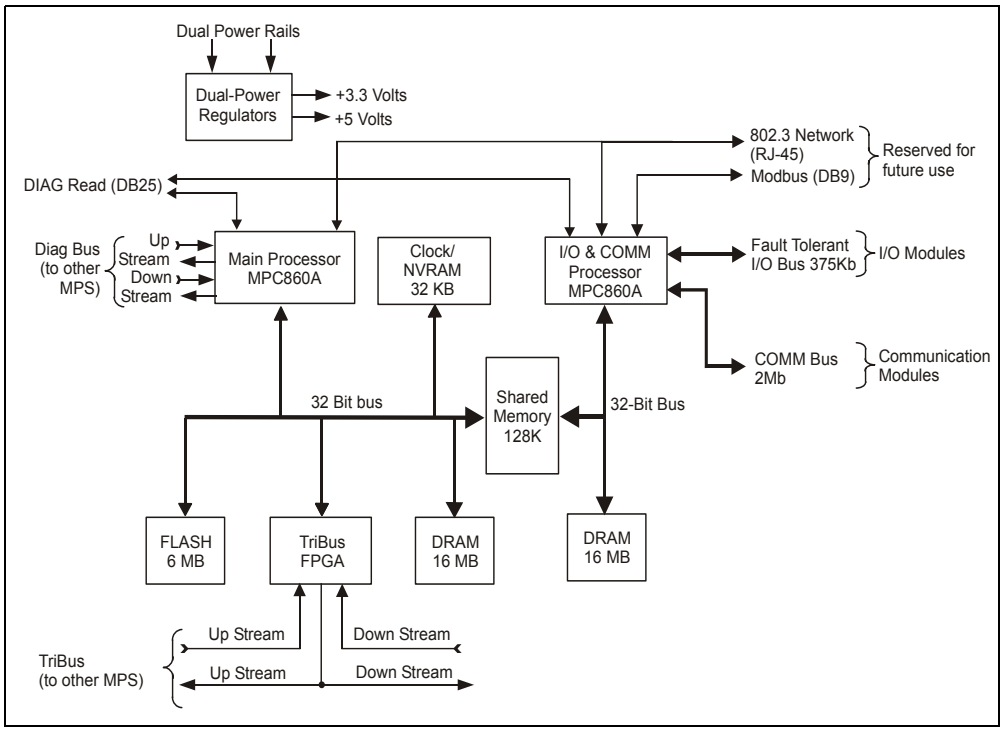
Bus Systems and Power Distribution

Three triplicated bus systems are etched on the chassis backplane: the TriBus, the I/O bus and the communication bus.

The TriBus consists of three independent serial links which operate at 25 megabits per second. The TriBus synchronizes the main processors at the beginning of a scan. Then each main processor sends its data to its upstream and downstream neighbors. The TriBus performs one of two functions with the data:

- Transfer of data only—for I/O, diagnostic and communication data.
- Comparing data and flagging disagreements—for the previous scan's output data and memory of user-written control program.

An important feature of the Tricon's fault-tolerant architecture is the use of a single transmitter to send data to both the upstream and downstream main processors. This ensures receipt of the same data by the upstream processor and downstream processor.



Main Processor (Model 3008) Architecture

I/O Bus

The triplicated I/O bus transfers data between the I/O modules and the main processors at 375 kilobits per second. The triplicated I/O bus is carried along the bottom of the backplane. Each channel of the I/O bus runs between one of the three main processors and the corresponding channels on the I/O module.

The I/O bus can be extended between chassis using a set of three I/O bus cables.

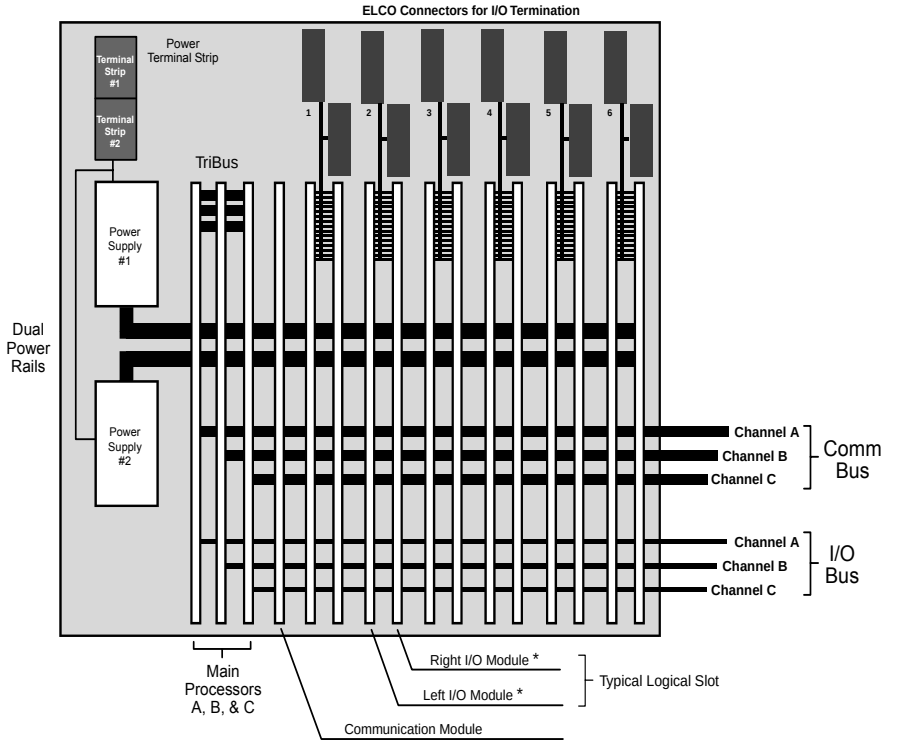
Communication Bus

The communication (COMM) bus runs between the main processors and the communication modules at 2 megabits per second.

Power for the chassis is distributed across two independent power rails down the center of the backplane. Every module in the chassis draws power from both power rails through dual power regulators. There are four sets of power regulators on each input and output module: one set for each of the channels A, B and C and one set for the status-indicating LED indicators.

Field Signals

Each I/O module transfers signals to or from the field through its associated field termination assembly. Two positions in the chassis tie together as one logical slot. The first position holds the active I/O module and the second position holds the hot-spare I/O module. Termination cables are connected to the top of the backplane. Each connection extends from the termination module to both active and hot-spare I/O modules. Therefore, both the active module and the hot-spare module receive the same information from the field termination wiring.



Backplane of the Main Chassis

Digital Input Modules

The Tricon supports two basic types of digital input modules: TMR and single. The following paragraphs describe digital input modules in general, followed by specifics for TMR and single modules.

Every digital input module houses the circuitry for three identical channels (A, B and C). Although the channels reside on the same module, they are completely isolated from each other and operate independently. A fault on one channel cannot pass to another. In addition, each channel contains an 8-bit microprocessor called the I/O communication processor, which handles communication with its corresponding main processor.

Each of the three input channels asynchronously measures the input signals from each point on the input termination module, determines the respective states of the input signals, and places the values into input tables A, B and C respectively. Each input table is regularly interrogated over the I/O bus by the I/O communication processor located on the corresponding main processor module. For example, Main Processor A interrogates Input Table A over I/O Bus A.

On TMR digital input modules, all critical signal paths are 100 percent triplicated for guaranteed safety and maximum availability. Each channel conditions signals independently and provides isolation between the field and the Tricon. (The 64-point high-density digital input module is an exception—it has no channel-to-channel isolation.)

DC models of the TMR digital input modules can self-test to detect stuck-ON conditions where the circuitry