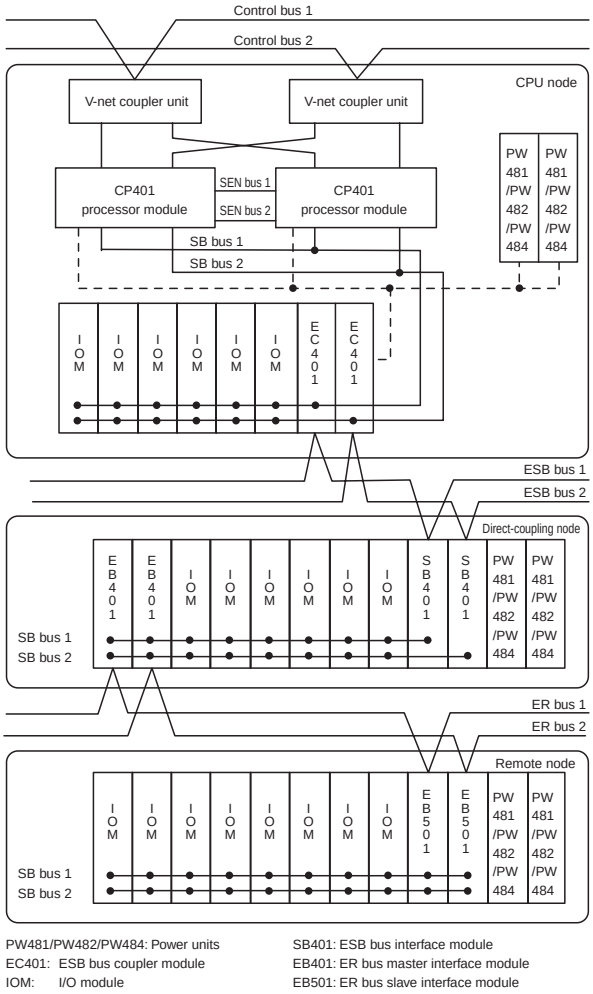

Figure 4 Configuration of Dual-redundant FFCS

R3 have been made common to each other. This section focuses on the hardware of the newly developed CPU node.

CPU Node

A maximum of eight IOMs can be installed in the CPU node, allowing the CPU node to operate alone as the minimum system of the FFCS.

A maximum of three extension nodes (direct-coupling and remote nodes) can be connected to the CPU node. When connecting the CPU node and direct-coupling node, an ESB bus coupler module (EC401) is installed in the IOM section of the CPU node and an ESB bus slave interface module (SB401) is installed in the extension node. When using the remote node in place of the extension node, an ER bus master interface module (EB401) is installed in the IOM section of the CPU node or direct-coupling node.

Processor Module (CP401)

Figure 5 shows the dual-redundant configuration of the processor modules. The dual-redundant processor modules employ the field-proven Pair & Spare method. Each processor module comprises two MPUs, where the MPUs perform the same control computations and the computation results are cross-checked by the collators to detect transient errors. With the dual redundancy of processor modules, the transfer of the control right in case of system failure and the continuation of control are accomplished without any momentary shutdown, achieving high degrees of system availability.

Figure 6 shows the external view of the processor module. The module has been changed in shape from the conventional card-like form to a modular form in which the internal assembly is encapsulated in a molded housing. For the internal hardware configuration, we reused the hardware assets, i.e., the processor

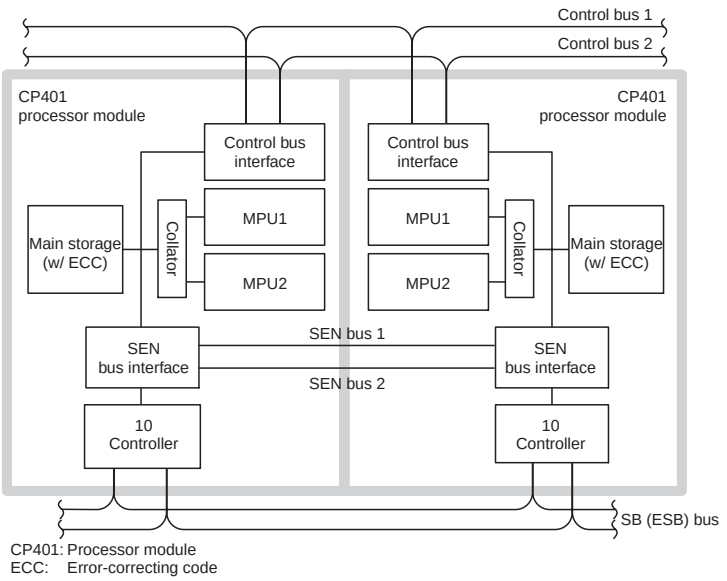

Figure 5 Configuration of Dual-redundant CP401 Processor Modules

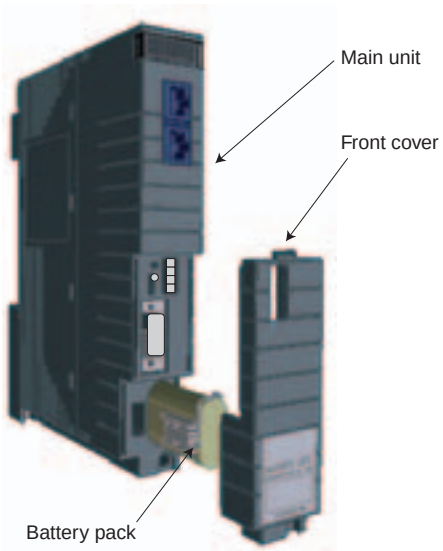

Figure 6 External View of CP401 Processor Module

Table 1 Brief Specifications of SEN Bus

Item	Remarks
Transmission method	Synchronous serial transmission
Data access size	Dependent on the frame (1 to 256 bytes)
Data simultaneity	Guaranteed within the frame
Address space	32 bits within each module (4 GB)
Transmission rate	384 Mbps
Error detection	CRC-CCITT (16 bits)
Topology	Point-to-point
Number of master modules	2 max.
Bus signal level	LVDS, EIA/TIA-644
Bus redundancy	Standard feature
Connection/disconnection of modules with the line electrified	Supported

card (CP345) and SB bus interface card (SB301) of the industry-proven CENTUM CS3000, and incorporated them into a single module, while maintaining the software compatibility as much as possible. Equipped with the microprocessor which is field-proven as has been used for the industry-proven CP345 processor card, the processor module makes it possible to build scalable systems by using the same system software for small- to medium-scale plants and large-scale plants as well.

In order to mount the CP345 and SB301 on a single module (i.e., to achieve downsizing), we actively adopted a programmable device in a fine-pitched multi-pin ball grid array (BGA) as a large-scale integration component, chip capacitors and resistors of 1005 size as small-size components, and new elemental technologies, including build-up boards for densely mounting such components.

The processor module contains a battery pack in order to back up the main memory in case of power failure. However, taking environmental protection into consideration, the conventional nickel-cadmium batteries have been abandoned and replaced with nickel-hydrogen batteries.

SEN Bus

We have also developed the SEN bus for program copying and data equalization between the processor modules. Table 1 shows the specifications of the SEN bus in brief.

Traditionally, data exchange between the processor modules has been performed using a parallel transmission method. In the case of the SEN bus however, the method has been replaced with the point-to-point high-speed serial transmission method to reduce the mounting area and the number of signal lines to one-tenth those of the conventional bus. Since the LVDS (EIA/TIA-644 standard) method featuring small signal amplitudes has been adopted for the bus signal levels, radiation noise has been reduced and power consumption has also been dramatically reduced. From the point of view of high reliability, we added an error-detecting code and made it possible to connect/disconnect the module with the line electrified. The SEN bus is provided with error-detecting functions, such as constantly performing self-diagnoses using idle frames even in the absence of bus access requests. From a software point of view, the SEN bus inherits exactly the same interface as that of the existing backplane bus. Thus the FFCS features a design in which users need not be conscious of the SEN bus.

ESB Bus Coupler Module (EC401)

We have also developed the ESB bus coupler module (EC401) designed to connect the direct-coupling node to the CPU node. The module has one port for the ESB bus to communicate with the ESB bus interface module (SB401). By installing two units of the module, it is possible to support for the dual redundancy of the ESB bus.

V-net Coupler Unit

The FFCS employs the field-proven V-net as the control bus. The V-net coupler unit is equipped with a V-net data link control section and physical layer interface to provide signal isolation and level conversion for the V-net.

CONCLUSION

Yokogawa Electric's DCSs have evolved through the positive adoption of new technologies in line with market requirements (performance, functionality, and capacity increase). We have increased the capacity and functionality of FCSs' control units in harmony with improvements in semiconductor integration technology and enhancements in microprocessor performance. Since the amount of data for equalization between the dual-redundant processors has increased significantly, the conventional transfer capacity will no longer suffice.

We have retrofitted the backplane bus which has not been changed since the release of the CENTUM CS. In addition, we have developed the SEN bus (high-speed serial bus) for data equalization between the dual-redundant processor modules of the FFCS. The technical progress of the SEN bus holds promise for the bus to become even faster in future. Consequently, it will become possible to further enhance the functionality and performance of FCSs. ◆

REFERENCES

(1) Matsuda Toshihiko, Sano Hideo, Soggo Sadatoshi, Hazama Meguru, “Fault Tolerant Design for Field Control Stations”, Yokogawa Technical Report , Vol. 18, 1994, pp. 10-13

(2) Komiya Hiroyoshi, Akai Hajime, Matsuda Toshihiko, Nishida Jun, “Fault Tolerance of Distributed Process Control Systems”, The Institute of Electronics—Information and Communication Engineers Technical Research Report, Vol. 97, No. 98, 1997, pp. 35-40 (in Japanese)

(3) Kato Eiji, Nakamoto Eiji, Matsuda Toshihiko, “Features of Field Control Station Hardware”, Yokogawa Technical Report, No. 26, 1999, pp. 6-9