GEH-6723P

Mark* VIeS Safety Control

Functional Safety Manual

Feb 2018

For public disclosure

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Document Updates

Revision	Location	Description
P	*Controller Application Code*	Added approval for SIL3 use per IEC 61508–3
	Critical System Timing Parameters	Added 10 ms frame period to critical system design parameters
	Maximum Remote I/O Stimulus to Response Time	Clarified the Mark VIeS maximum remote I/O Stimulus to Response Time calculation
	Restrictions	Added additional restrictions for 10 ms frame period for controllers
	Product Life	Added UCSCS2A to second bullet item concerning wear items
	Appendix: Determine Frame Input Client Completion Time	Added appendix with procedures to determine frame input completion time with Mark VIeS V06.00 (ControlST V07.02).
N	*SIF Function Blocks* table	Added new SIL Blocks
	Branding	Branding is needed after upgrades from BPPB to BPPC based I/O packs
	YTCC Configuration table	Corrected YTCC SysLimit1 and SysLimit1 choices temperature range
	YTCC Cold Junctions table	Corrected YTCC Cold Junction TMR_DiffLimit choices temperature range
M	YSIL Test Procedures	New *TCSA ETR#_Open Test*
	I/O Configuration	Added *Output Bits* in the YSIL configuration *YTCC*, *YAICS1B*, *YDIAS1B*: updated to be in sync with GEH-6721_Vol_II Added firmware compatibility information to *YVIB*, YAIC, YDIA, and *YDOA*
L	I/O Configuration	New section, *YSIL* YDOA, updated to be in sync with GEH-6721_Vol_II
	Table, *Process I/O Packs*	Added SRSA
	Figure, *Turbine Protection with YTUR and YPRO*	Corrected YPRO trip board to be TREG
	The section, *Application-specific I/O*	Added YSIL
	Proof Tests	Added *YSIL Proof Test Requirements* and *YSIL Test Procedures*
	YDOA Test Procedures	Updated to include SRSA
	Locked Mode	Provided a more general description
	Black Channel	Moved this information into GEH-6721_Vol_II
	Throughout	Updated to define differences in YVIBS1A and the new YVIBS1B
	The table, *SIF Function Blocks*	Added a Caution to indicate blocks that are not currently available for SIFs.

Acronyms and Abbreviations

BPCS	Basic process control system
CRC	Cyclic redundancy check
DC	Diagnostic coverage
EGD	Ethernet global data
ETD	Electrical trip device
EUC	Equipment under control
HFT	Hardware fault tolerance
IEC	International Electrotechnical Commission
LOP	Layers of protection
MTTFS	Mean time to fail spurious
PDM	Power distribution module
PT	Potential transformer
PTI	Proof test interval
PFD_{avg}	Average probability of failure on demand
PFH	Probability of failure per hour
PST	Process safety time
RRF	Risk Reduction Factor
SIF	Safety-instrumented function
SIL	Safety integrity level
SIS	Safety-instrumented system
TMR	Triple modular redundancy

Related Documents

Doc #	Title	Description
GEH-6721_Vol_ I	Mark VIe and Mark VIeS Control System Guide	Provides an overview of the Mark VIe and Mark VIeS control systems. The *Technical Regulations, Standards, and Environments* chapter provides a list of applicable agency codes and standards.
GEH-6721_Vol_II	Mark VIe and Mark VIeS Control System Guide	Describes all of the hardware elements that are available for use in a Mark VIeS control
GEH-6721_Vol_III	Mark VIe and Mark VIeS Control System Guide	Describes all of the hardware elements that are available for use in a Mark VIeS control
GEH-6703	ToolboxST User Guide for Mark Controls Platform	Contains instructions for using the ToolboxST application to configure and control a Mark VIeS system
GEI-100691	Mark VIe Safety Integrity Level (SIL) Block Library	Documents the controller blocks available in a Mark VIeS control
GEH-6808	ControlST Software Suite How-to Guides	Provides procedures for setup and configuration of Mark VIeS components
IEC 61508	Functional Safety of Electrical/Electronic/Programmable Electronic Safety-related Systems	
IEC 61511	Functional Safety – Safety Instrumented Systems for the Process Industry Sector	

Safety Symbol Legend

Warning

Indicates a procedure or condition that, if not strictly observed, could result in personal injury or death.

Caution

Indicates a procedure or condition that, if not strictly observed, could result in damage to or destruction of equipment.

Attention

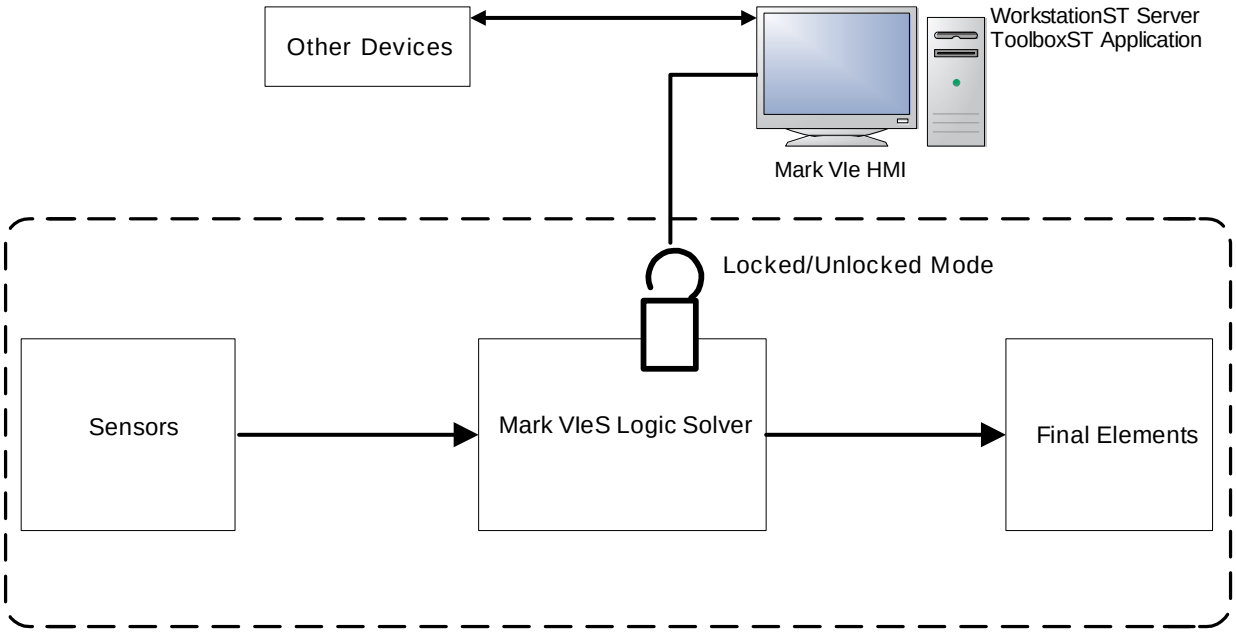
Indicates a procedure or condition that should be strictly followed to improve these applications.

Contents

1 Introduction

The Mark* VIeS Safety control is a stand-alone safety control system used by operators knowledgeable in safety-instrumented system (SIS) applications to reduce risk in critical safety functions. It is a derivative of the Mark VIe control system used in a variety of power plant applications. The Mark VIeS Safety control is programmed and configured with the same ToolboxST* application that is used in the Mark VIe control. The Mark VIeS Safety controller and distributed I/O module firmware are enhanced for safety control use. Specific Mark VIe control hardware has also been identified for use in safety control systems.

While the Mark VIeS control performs the logic solving tasks for the system, it can also interface with the ToolboxST application. The ToolboxST application can interface with an external distributed control systems (DCS). It provides a means to lock or unlock the Mark VIeS control for configuration and safety-instrumented function (SIF) programming. This allows you to install a safety function, test it, and place the controller in *Locked* mode to perform safety control.



Mark VIeS Control as Part of a SIS

Interfaces to the Mark VIeS control must be strictly controlled to avoid interference with the operation of the system. Data exchange to the safety control must be restricted and only used when validated by the application software.

The Mark VIeS control was designed and certified to meet functional safety standards according to *IEC 61508* Parts 1 through 3. It is certified for use in both high-and low-demand applications. The Mark VIeS control uses redundant architecture configurations and a hardware fault tolerance (HFT) of 1 to achieve safety integrity level (SIL) 3. The highest achievable SIL with an HFT of 0 is SIL 2.

Notes

2 Functional Safety

IEC 61508-4 definitions are as follows:

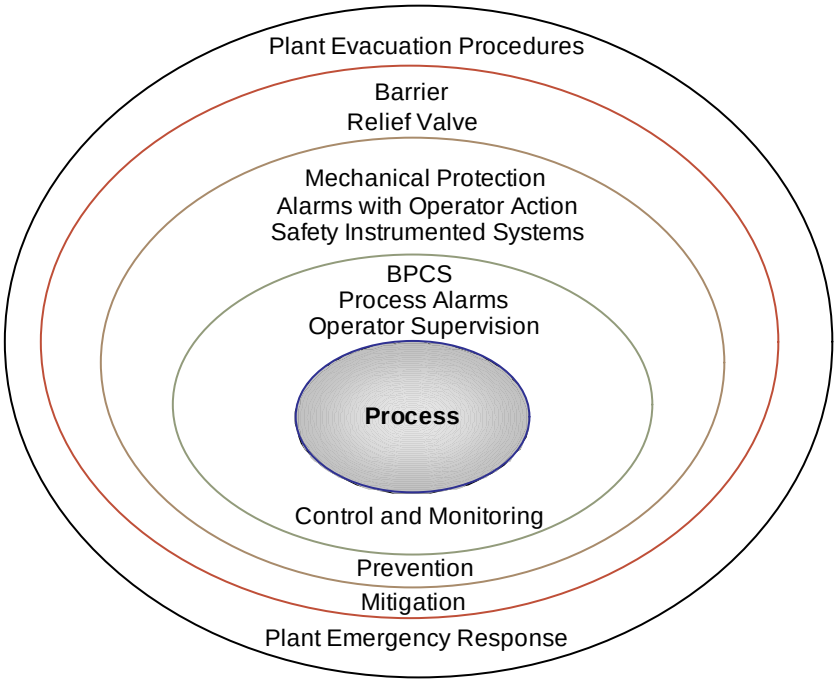
Safety Freedom from unacceptable risk.

Risk Combination of the probability of occurrence of harm and the severity of that harm.

Functional Safety Part of the overall safety relating to the equipment under control (EUC) and the EUC control system that depends on the correct functioning of the Electrical/electronic/programmable electronic (E/E/PE) safety-related systems, other technology safety-related systems, and external risk reduction facilities.

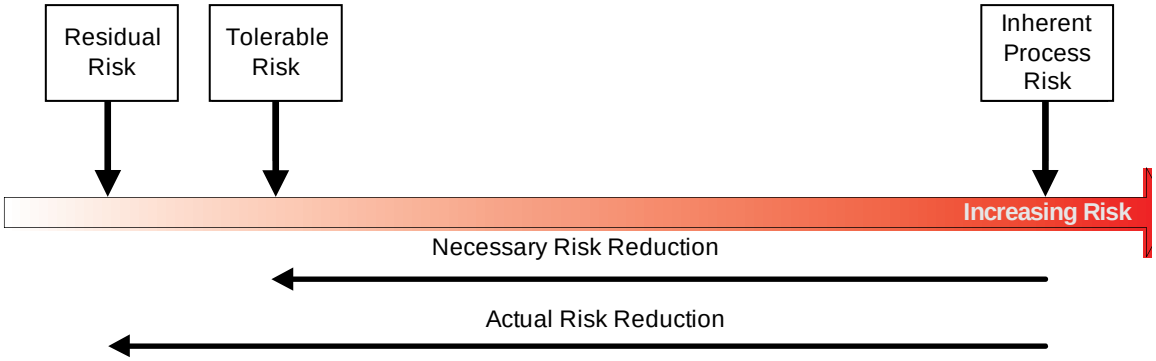
2.1 Risk Reduction

Functional safety relates to proper equipment operation, as well as other risk reduction facilities. Layers of protection (LOP) concepts are as follows:



LOP

The LOP around a process can be used to introduce risk reduction. Failure to carefully analyze the available LOP and the likelihood-consequence relationship of the risks involved with process control failure can lead to an expensive over-design of the system. The goal is to reduce the risk to a level that is as low as reasonably practicable (ALARP).



To achieve functional safety, it is necessary to analyze the potential hazards to personnel and property, including any environmental impact, that could occur when the control of equipment is lost.

Requirements for safety function and integrity must be met to achieve functional safety. Safety function requirements describe what the safety function does and is derived from the hazard analysis. The safety integrity requirement is a quantitative measure of the likelihood that a safety function will perform its assigned task adequately. For safety functions to be effectively identified and implemented, the system as a whole must be considered.

A primary parameter used in determining the risk reduction in a safety controller is the Average Probability of Failure on Demand (PFD_{avg}). The inverse of the PFD_{avg} is the Risk Reduction Factor (RRF).

$$RRF = \frac{1}{PFD_{avg}}$$

2.1.1 Modes of Operation

A demand mode is a mode operation in which the safety function is called upon only on demand. *IEC 61508-4* clause 3.5.12 defines two demand modes of operation:

- Low demand mode
- High demand or continuous mode

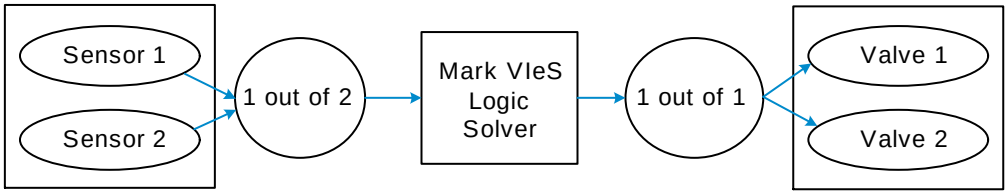
Low demand describes the mode in which safety function demand occurs no greater than once per year and no greater than twice the proof test frequency. In high demand mode, the frequency of demand is greater than once per year or greater than twice the proof test frequency. Continuous mode is regarded as very high demand and is associated with the safety function operating to keep the EUC within its normal safe state.

The mode of operation is relevant when determining the target failure measure of a safety function. Low demand mode relates to the PFD_{avg} whereas high demand or continuous demand mode relates to measuring the probability of failure per hour (PFH) (there are approximately 10^4 hours in a year). IEC 61508 defines a scale of four distinct levels of risk reduction referred to as the Safety Integrity Level (SIL).

SILs

SIL	PFD_{avg} Low Demand Mode	PFH High Demand Mode	RRF
1	≥ 10^{-2} to < 10^{-1}	≥ 10^{-6} to < 10^{-5}	> 10 to ≤ 100
2	≥ 10^{-3} to < 10^{-2}	≥ 10^{-7} to < 10^{-6}	> 100 to ≤ 1,000
3	≥ 10^{-4} to < 10^{-3}	≥ 10^{-8} to < 10^{-7}	> 1,000 to ≤ 10,000
4	≥ 10^{-5} to < 10^{-4}	≥ 10^{-9} to < 10^{-8}	> 10,000 to ≤ 100,000

The SIL applies to all elements in the safety loop (sensors, logic solver, and final element) and their architecture. The loop must be considered in its entirety.



Safety Loop

2.2 Hazard and Risk Analysis

Hazard and risk analyses determine the necessary safety functions and the required levels of risk reduction (refer to *IEC 61508-5:1998*). The recommended safety life cycle stipulates the completion of a hazard and risk analysis early in the process.

A hazard analysis, the identification of potential sources of harm, determines the causes and consequences of hazardous events. A team of professionals, familiar with both the EUC and safety-related systems, typically conducts the hazard analysis.

A risk analysis is typically defined in three stages: hazard identification, hazard analysis, and risk assessment. Risk analysis, like hazard analysis, requires a large spectrum of expertise and a team effort is required to produce a viable result. Annexes A – F of *IEC 61511-3* provides guidance in producing a risk analysis.

2.3 Safety Life Cycle

The safety life cycle is crucial to the philosophy of functional safety. The safety life cycle involves the following recommended stages:

1. Functional safety management including functional safety assessment
2. Safety life cycle structure and planning
3. Hazard and risk analysis
4. Allocation of safety functions to protection layers
5. Safety requirements specification for the safety control
6. Design and engineering of safety control
7. Design and development of other means of risk reduction
8. Installation, validation, and commissioning
9. Operation and maintenance
10. Modification and retrofit
11. Decommissioning

IEC 61511 defines how to use the safety life cycle to achieve the desired SIL. Although the safety life cycle is described here and in *IEC 61511* as a sequence of stages, in practice it is a repetitive process. If, for example, a modification is required in the operational system, an impact analysis is required and the design changes should be reassessed starting with the hazard and risk analysis phase. Furthermore, for each safety function a hazard and risk analysis is required to define the safety function requirements and required SIL.

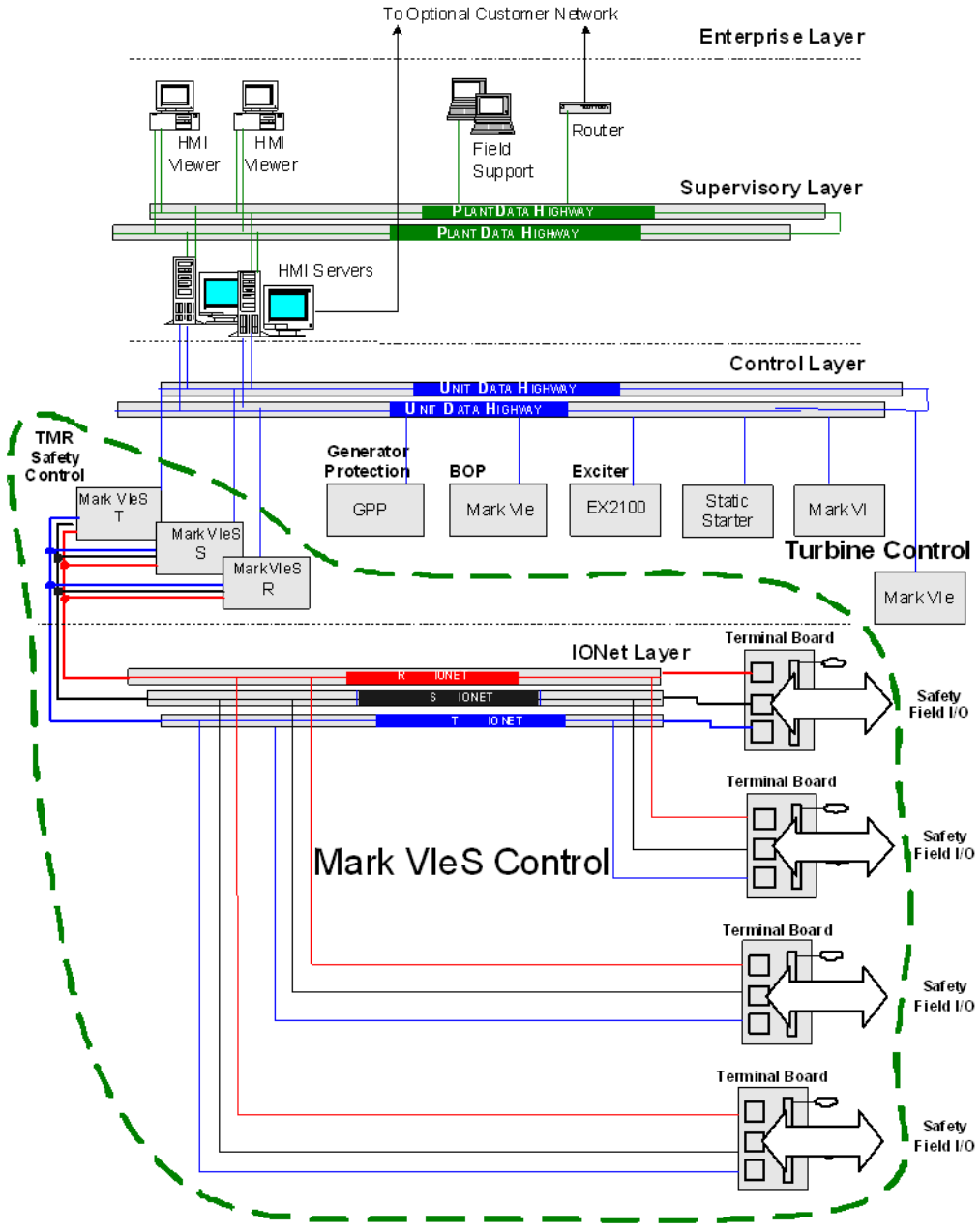
2.4 Functional Safety Management

Functional safety must be managed during the entire time of the safety life cycle. *IEC 61511* clause 5 describes the objectives and requirements for the management of functional safety. The functional safety management plan should be a formal document that outlines the activities related to functional safety and the persons in the organization responsible for those activities. It should also include functional safety assessment and audit planning.

IEC 61508 provides additional guidance about completing an effective functional safety management plan. The tables of technique and measures in Annex A and B of *IEC 61508* Tab 1, 2, and 3 are particularly useful.

3 System Design

This chapter describes the components that are critical to system implementation. The internal structure of the Mark VIeS control is displayed in the following figure.



Mark VIeS Safety Control within Entire Application

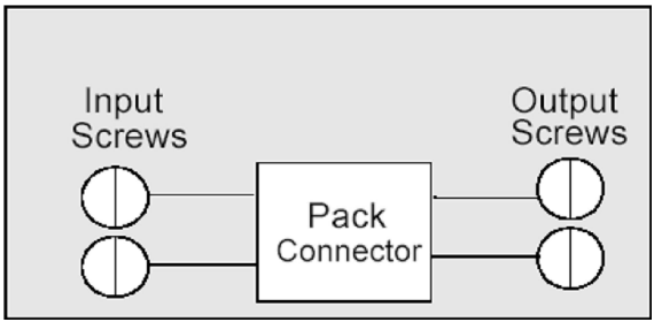
3.1 Primary Architecture Components

A Mark VIeS control for any supported architecture is built using a common set of safety approved components connected by a combination of direct wiring and the *IONet* communications bus. The Mark VIeS I/O signal path consists of three basic parts: terminal board, I/O pack, and IONet.

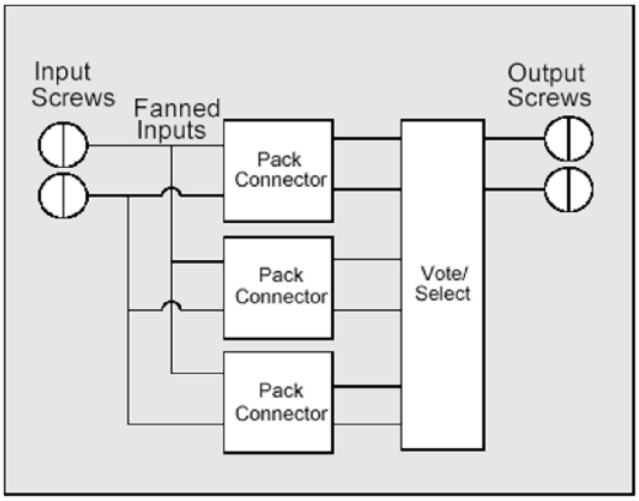
3.1.1 Terminal Boards

Terminal boards mount on the cabinet and are of two basic types: S and T. The S-type board provides wire terminals for each I/O point and allows a single I/O pack to condition and digitize the signal. This terminal board is used for simplex, dual, and dedicated triple modular redundant (TMR) inputs and outputs by using one, two, or three boards. The T-type is a fanned TMR board that typically fans the inputs to three separate I/O packs. For outputs, the T-type hardware provides a mechanism to vote the outputs from the three I/O packs.

Note Some application-specific TMR terminal boards do not fan inputs or vote the outputs.



Simplex Terminal Board



TMR Terminal Board

Both S-type and T-type terminal boards provide the following features:

- Terminal blocks for I/O wiring
- Mounting hardware
- Input transient protection
- I/O pack connectors
- Unique electronic ID

The following terminal board interfaces are available for field I/O:

Board	Typical Process I/O	# of Packs/Board
TBCIS1C	24 discrete inputs (125 V dc, group isolated)	1 or 2 or 3
TBCIS2C	24 discrete inputs (24 V dc, group isolated)	1 or 2 or 3
TBCIS3C	24 discrete inputs (48 V dc, group isolated)	1 or 2 or 3
STCIS1A, S2A	24 discrete inputs (24 V dc, group isolated)	1
STCIS4A	24 discrete inputs (48 V dc, group isolated)	1
STCIS6A	24 discrete inputs (125 V dc, group isolated)	1
TRLYS1B	12 Form C mechanical relays w/ 6 solenoids, coil diagnostics	1 or 3
TRLYS1D	6 Form A mechanical relays for solenoids, solenoid impedance diagnostics	1 or 3
TRLYS1F	36 mechanical relays, 12 voted form A	3
TRLYS2F	36 mechanical relays, 12 voted form B	3
SRLYS1A, S2A	12 Form C mechanical relays-dry contacts	1
SRSAS1A, S3A	Two banks of 5 channels each, for 10 total relay outputs	1
TVBAS1A, S2A	8 vibration or position, 4 position only, 1 reference (Keyphasor* transducers)	1 or 3
TBAIS1C	10 analog inputs (V and I) and 2 analog outputs 4-20 mA	1 or 3
STAIS1A, S2A	10 analog inputs (V and I) and 2 analog outputs 4-20 mA	1
SHRAS1A, S2A	10 analog inputs (V and I) and 2 analog outputs 4-20 mA, HART® capable	1
TBTCS1B	12 thermocouples	1 or 2 or 3
TBTCS1C	24 thermocouples (12 per I/O pack)	1
STTCS1A, S2A	12 thermocouples	1

Board	Application-specific I/O	# of Packs/Board
TTURS1C	Mixed I/O: 4 speed inputs/ pack	1 or 3
TRPAS1A	Speed inputs, trip outputs at 24 V dc, E-Stop	3
TRPAS2A	Speed inputs, trip outputs at 125 V dc, E-Stop	3
TRPGS1B	Primary trip – Gas, flame detector inputs	3 (through TTUR/YTUR)
TRPGS2B	Primary trip – Gas, flame detector inputs	1 (through TTUR/YTUR)
TREGS1B	Backup trip at 125 V dc, E-Stop	3 (through SPRO/YPRO)
TREGS2B	Backup trip at 24 V dc, E-Stop	3 (through SPRO/YPRO)
TREAS1A	Mixed I/O: 3 speed inputs, trip contacts at 24 V dc	3
TREAS2A	Mixed I/O: 3 speed inputs, trip contacts at 125 V dc	3
TREAS3A	Mixed I/O: 3 speed inputs, trip contacts at 24 V dc	3
TREAS4A	Mixed I/O: 3 speed inputs, trip contacts at 125 V dc	3
SPROS1A	Mixed I/O: 3 speed inputs, trip contacts	1

3.1.2 I/O Packs

Mark VIeS I/O packs contain a common processor board and a data acquisition board that is unique to the type of device to which it is connected. I/O packs on each terminal board digitize signals, perform algorithms, and communicate with the Mark VIeS controller. I/O packs provide fault detection through special circuitry in the data acquisition board and software running in the CPU board. The fault status is transmitted to, and used by, the controllers. Each I/O pack transmits inputs and receives outputs on both network interfaces if connected.

3.1.2.1 Process I/O

Typical process inputs include contact, analog, and thermocouple signals. Typical process outputs include relays and analog outputs. All typical process outputs based on inputs are processed by the system controller. The following process I/O packs are available for use in the Mark VIeS control:

Process I/O Packs

I/O Pack	Associated Terminal Board(s)	Functions	Redundancy
YAIC	TBAI, STAI	10 analog inputs (voltage, 4-20 mA) 2 analog outputs (4-20 mA)	1 or 3 packs
YDIA	TBCI, STCI	24 discrete inputs w/ group isolation (24 V dc, 48 V dc, or 125 V dc)	1, 2, or 3 packs
YDOA	TRLY_B, TRLY_F, SRLY TRLY_D	12 relay outputs 6 relay outputs	1 or 3 packs
	SRSA	10 relay outputs	1 pack
YHRA	SHRA	10 analog inputs (4-20 mA), 2 analog outputs (4-20 mA) (All I/O HART enabled)	1 pack
YTCC	TBTC, STTC	12 thermocouple inputs	1, 2, or 3 packs
YVIBS1A	TVBA	8 vibration, 4 position and 1 Keyphasor transducer	1 or 3 packs
YVIBS1B	TVBA	8 vibration, 3 position only, 2 position or Keyphasor	1 or 3 packs

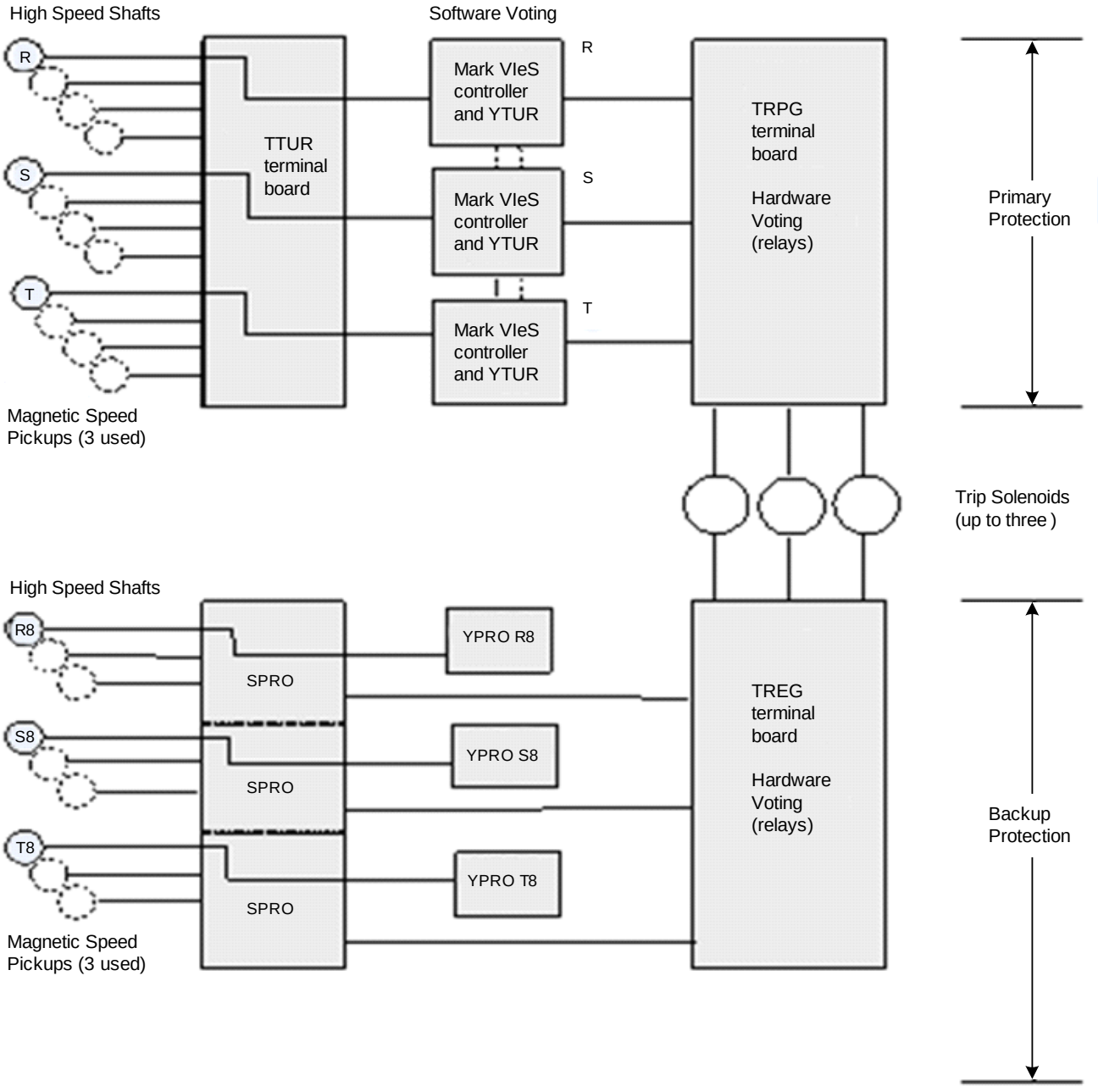
3.1.2.2 Application-specific I/O

Mark VIeS Safety control system includes GE application-specific functions. The ability to accept local inputs and drive local outputs independent of the system controller differentiates these from the typical process I/O. GE application-specific I/O types include pulse rate speed inputs and flame detectors. In the Mark VIeS control, the following application-specific I/O packs are available:

I/O Pack	Associated Terminal Board(s)	Functions	I/O Redundancy
YPRO	TREA, TREG, SPRO	Backup/emergency protection 3 speed inputs 7 contact inputs 3 monitored trip relay outputs 1 E-Stop	3 packs
YTUR	TTUR, TRPA, TRPG	Primary turbine protection 4 speed inputs 8 flame inputs 3 monitored trip relay outputs 1 E-Stop	1 or 3 packs
YSIL	Three I/O packs are mounted to TCSA + WCSA, which connects by serial links to three SCSAs to form the YSIL module	Core safety protection Refer to table, *YSIL I/O Functions*	3 packs

The YPRO, YTUR, and YSIL process speed signals and operate trip relays locally, without requiring controller participation. The compatible mating terminal boards detect the correct operation of the tripping relay output circuits. YTUR includes a non-certified but non-interfering capability to synchronize a generator to a utility grid and control a connection breaker. The YPRO and YSIL include a non-interfering backup synchronizing check.

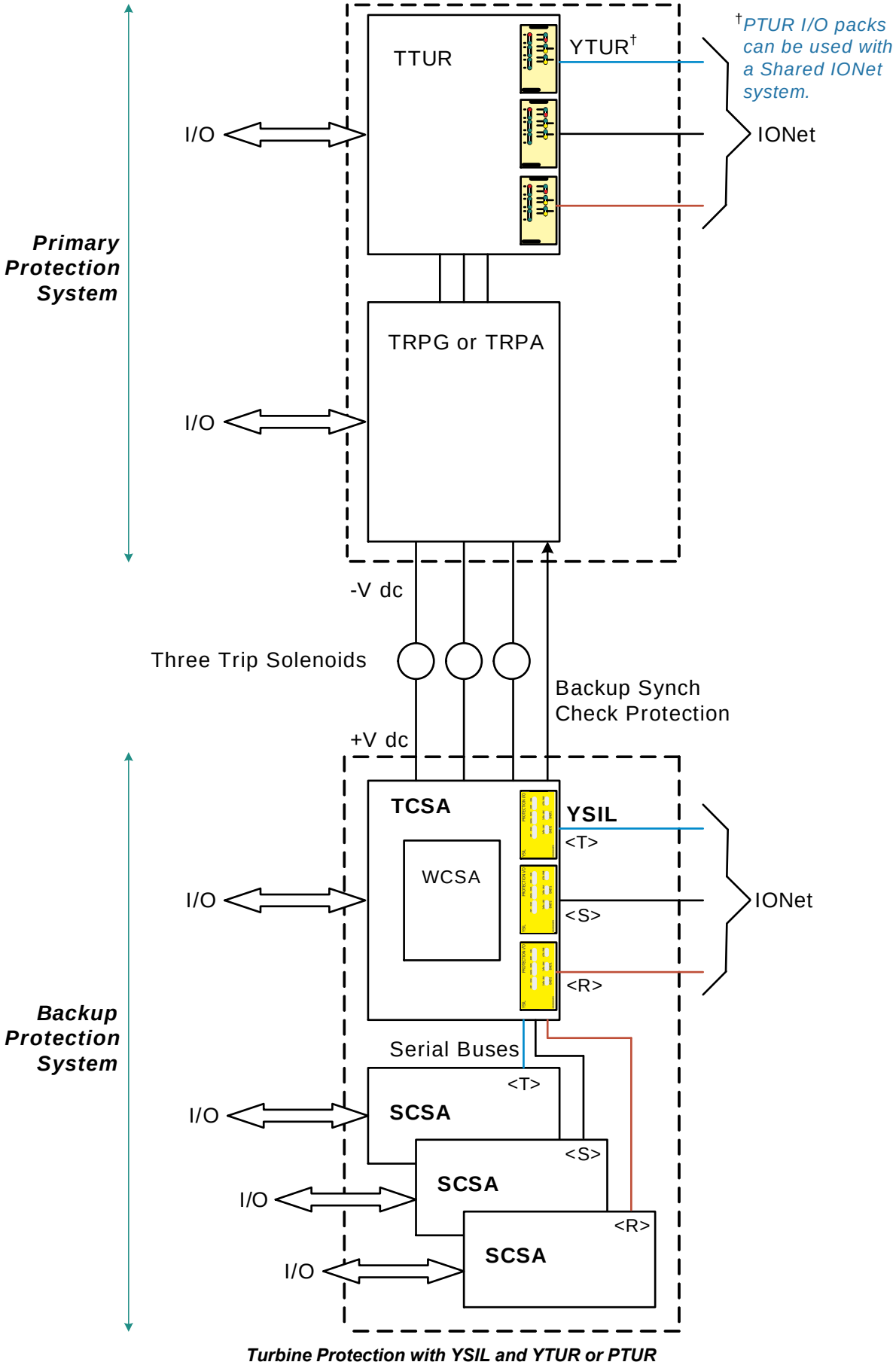
Turbine overspeed protection is available as follows: control, primary, and backup. The controller provides primary overspeed protection. The TTUR terminal board and YTUR I/O pack carry a shaft speed signal to each controller, which select the median signal. If the controller finds a trip condition, it sends the trip signal to the TRPG terminal board through YTUR. A three-relay voting circuit (one for each trip solenoid) performs a two out of three vote of the three YTUR outputs and removes power from the solenoids. The YPRO adds firmware and hardware based redundant overspeed protection.



Turbine Protection with YTUR and YPRO

YSIL I/O Functions

Signal Qty.	Description	Redundancy	Board
33	4-20 mA, 2-wires, loop powered (11 inputs times three SCSAs)	Simplex	SSCA
18	4-20 mA, 2–wires, externally powered (6 inputs times three SCSAs)	Simplex	SCSA
6	Contact outputs (2 outputs times three SCSAs)	Simplex	SCSA
9	Contact inputs, 24 V dc powered (3 inputs times three SCSAs)	Simplex	SCSA
1	Emergency push-button dedicated discrete input, capable of initiating a TRIP output without firmware interaction (hardware trip)	TMR Voted	TCSA
17	Contact inputs, 24 V dc powered, firmware trip option	TMR Fanned	TCSA
8	Flame detector Honeywell type inputs	TMR Fanned	TCSA
10	Flame detector externally powered 4-20 mA inputs (Rueter Stokes)	TMR Fanned	TCSA
6	Gas compressor speed probes (magnetic pickup and TTL option) ‡ Dual sensor 3-shaft or Triple sensor 2-shaft configurations	‡	TCSA
6	Gas compressor speed probes repetitions (individually shielded, RS-232/485 options)	‡	TCSA
3	Contact inputs, 24 V dc powered	TMR Fanned	TCSA
3	Solenoid out, 24 V dc or 125 V dc General purpose or optionally configured as Energize to Trip (ETR) outputs	TMR Voted	TCSA
6	Solenoid out, 24 V dc or 125 V dc Energize to Trip (ETR) outputs	TMR Voted	TCSA
2	Contact output, voted configuration	TMR Voted	TCSA
2	Potential transformers for line/gen synchronization	TMR Fanned	TCSA



Turbine Protection with YSIL and YTUR or PTUR

3.1.3 IONet

The controllers and I/O packs communicate through the internal IONet (a closed network), using a proprietary IONet protocol. IONet communications are as follows:

- I/O packs that multicast inputs to the controllers each frame
- Controllers that broadcast outputs to the I/O packs each frame

3.2 Safety-instrumented Functions (SIF)

Mark VIeS SIF configurations are created and maintained in the ToolboxST application, along with the basic process control configurations. This environment provides all the facilities to create, download, and maintain these configurations.

Mark VIeS controllers have two operating modes for application execution. When in *Unlocked* mode, full access to the controller is granted, including the ability to download code, set constants, force points, and all other configuration and diagnostic operations. When in *Locked* mode, all changes to the controller operation are prevented to ensure the integrity of the safety functions.

Within the Mark VIeS controller, *branding* is used to support Locked mode and integrity checks. When the controller is unlocked and the operator is satisfied with the system operation, the system configuration is branded so that it can be uniquely identified. Once branded, a diagnostic alarm is generated if there are any changes to application code, constants, hardware integrity, or network connectivity. The diagnostics based on branding include all communications through the IONet to provide 100% network diagnostic coverage (DC) independent of the network hardware selected.

The typical sequence of application creation includes:

- Application development
- Hardware connection and configuration
- Function testing while unlocked
- Application branding (after being tested and proven)
- Placing the controller in Locked mode

3.2.1 Controller Application Code

Changes to the application code must be completely verified and tested prior to use in a SIF. The Mark VIeS Safety control provides several features to facilitate changes and track the state of application code acceptance. The following table lists the function blocks approved for SIL3 use per IEC 61508-3 that are available for use in SIFs.

SIF Function Blocks

Function Block	Description
AND	16-input logical AND
BLACK_RX	Allows the reception of an exchange of up to 32 variables from a dedicated black channel EGD page, send from another Mark VIeS Safety controller
BLACK_TX	Allows the transmission of an exchange of up to 32 variables from a dedicated black channel EGD page to be received by another Mark VIeS Safety controller
BFILT	Boolean filter with configurable pick-up and drop-out delays
CALC	8-input calculator that performs mathematical, trigonometric, and logarithmic functions
Capture	The Capture Data (CAPTURE) block collects multiple samples of 1 to 32 variables in a buffer that can be uploaded to ToolboxST application or the Data Historian for display and analysis.
Cause and Effect Matrix	The Cause and Effect Matrix is a new special task for the Mark VIeS Safety controller
_COMMENT	Nonfunctional comment block with page break
_COMMENT_BF	Nonfunctional comment block with page break
_COMMENT_NB	Nonfunctional comment block without page break
COMPARE	Multi-function numeric comparator
COMPHYS	Numeric comparator with hysteresis and sensitivity
COUNTER	Re-triggerable up counter
CTRLR_MON	Controller monitor
DEVICE_HB	Drives the heartbeat signal on the YPRO
EXPAND_UDI	32-input mapped bit expander
LATCH	Set and reset latch
LOGIC_BUILDER_SC	Allows up to 32 inputs to be configured with the AND, OR, and NOT blocks to create a PERMIT, OVERRIDE, FORCE, or TRACK type block
NOT	Logical inversion
ON_OFF_DELAY	Behaves as a switch with a delayed response, whether being turned on or off
OR	16-input logical OR
MEDIAN	3-input median selector
MOVE	Memory mover; data type translator
PREVOTE	Prevote values and health
PULSE	Boolean one-shot with programmable width
RUNG	16-input logic solver
SELECT	8-input selector
SYS_OUTPUTS	I/O system command output interface
TEMP_STATUS	Temperature sensing
TIMER	Re-triggerable up-count timer
TIMER_V2	Accumulates incremental time into CURTIME while RUN is True

SIF Function Blocks (continued)

Function Block	Description
UNIT DELAY	One frame delay line
VAR_HEALTH	Variable health status

Caution

Any block that is included in the SIL Block Library (GEI-100691.pdf) but is not listed in the previous table, *SIF Function Blocks* is not available for use in SIFs.

3.2.1.1 Variable Health

Inside the Mark VIeS Safety controller, every variable is associated with a set of qualities that provide additional information, or support advanced features such as forcing, simulation, or alarms. Some of these qualities are visible to users through ToolboxST application, and others are made available to application code through blockware.

Variable health measures the validity of the data stored in the variable. When the ToolboxST application collects variable data from the controller, it also scans the health information and displays a *U* (for unhealthy) beside each live data value if the corresponding health quality is FALSE. The Variable Health block (VAR_HEALTH) allows application code to access variable health. The Prevote block (PREVOTE) allows application code to access prevote values and health.

The health of a variable with no connection to I/O is always TRUE and therefore uninteresting. Also, output health is always TRUE. The health of variables associated with I/O is calculated from point and link health. *Point health* originates from software close to the hardware. *Link health* is calculated by the controller. These two values are passed through a logical AND gate to form variable health.

Each I/O server defines the non user-configurable point and group health. For example, the point health of an analog input may be declared unhealthy if its value exceeds some limit, and the point health of all inputs on an I/O pack may be declared unhealthy if a problem is detected in the signal acquisition hardware. It may not be practical for an I/O server to provide a health indication for each individual point and so this component of variable health is optional.

In a Mark VIeS Safety control, I/O is typically distributed at the I/O packs or across another network such as the Unit Data Highway (UDH). As such, the controller provides link health by validating that all transport layer checks between the I/O server and the controller are met. These may include timely delivery, signature matching, and checksums.

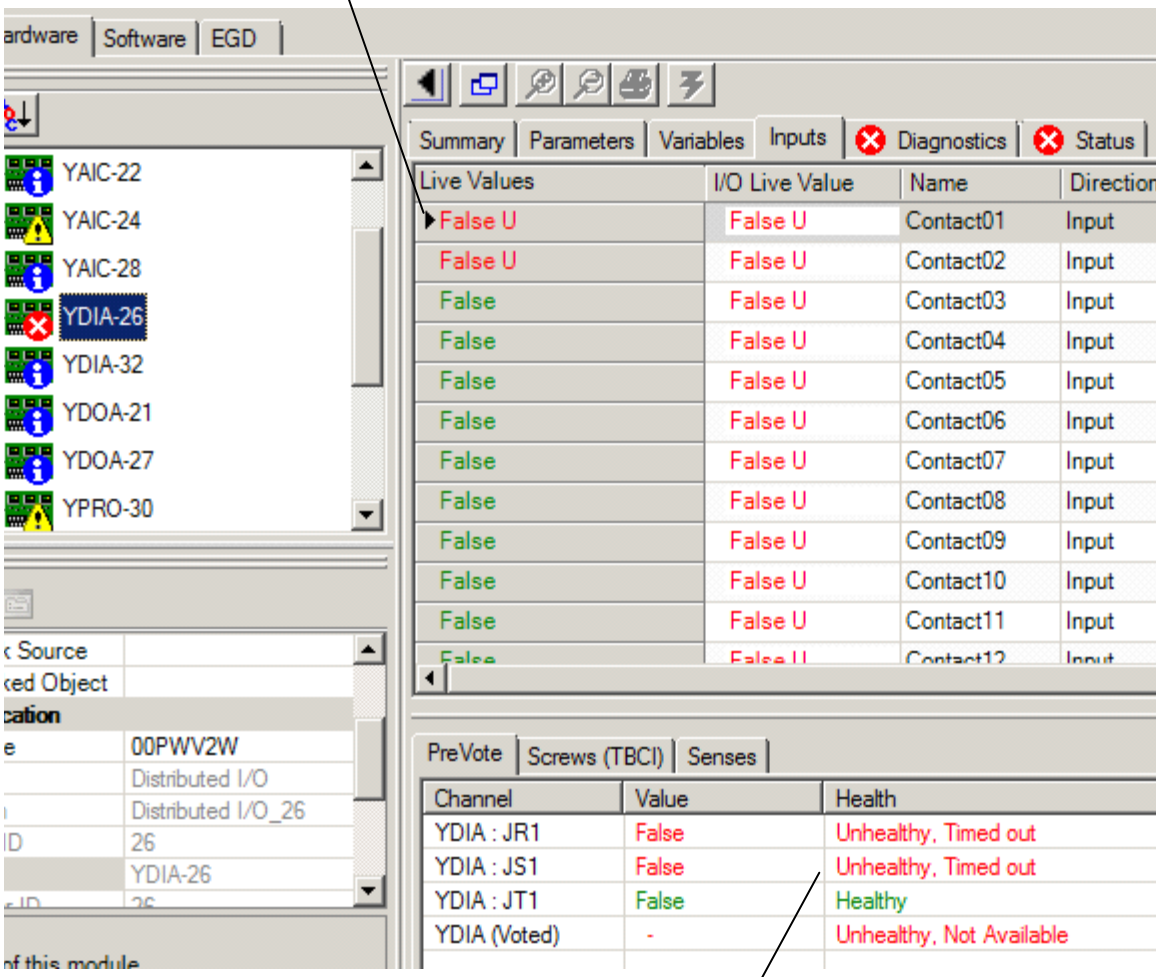
Redundant I/O features complicate the explanation of the variable health calculation. A TMR input module supplies three opinions of variable health to the controller. Since these inputs are voted, as long as two out of three are healthy, the resulting variable is also healthy.

A dual input module (either simplex I/O pack, dual network; or dual I/O pack, single network) provides two opinions of variable health to the controller. Since the controller cannot vote two opinions, it uses link health to select one of the channels and incorporates only the selected channel's point and group information into the variable health calculation. If the link health on the selected channel ever becomes unhealthy, the controller immediately switches to the second channel.

The VAR_HEALTH block reveals the variable health and the link health of the connected variable. Application developers can choose to monitor the health of individual variables or the health of the network (link) that supplies many variables, especially if the I/O on the other end of that network does not provide any additional health information. For TMR inputs, the link health pin provides a voted link health (that is, two out of three channels). For dual inputs, the link health pin provides the health of the selected channel.

The following ToolboxST screen displays a TMR YDIA with two faulted channels. Because of the faults, all points on the YDIA are marked as unhealthy.

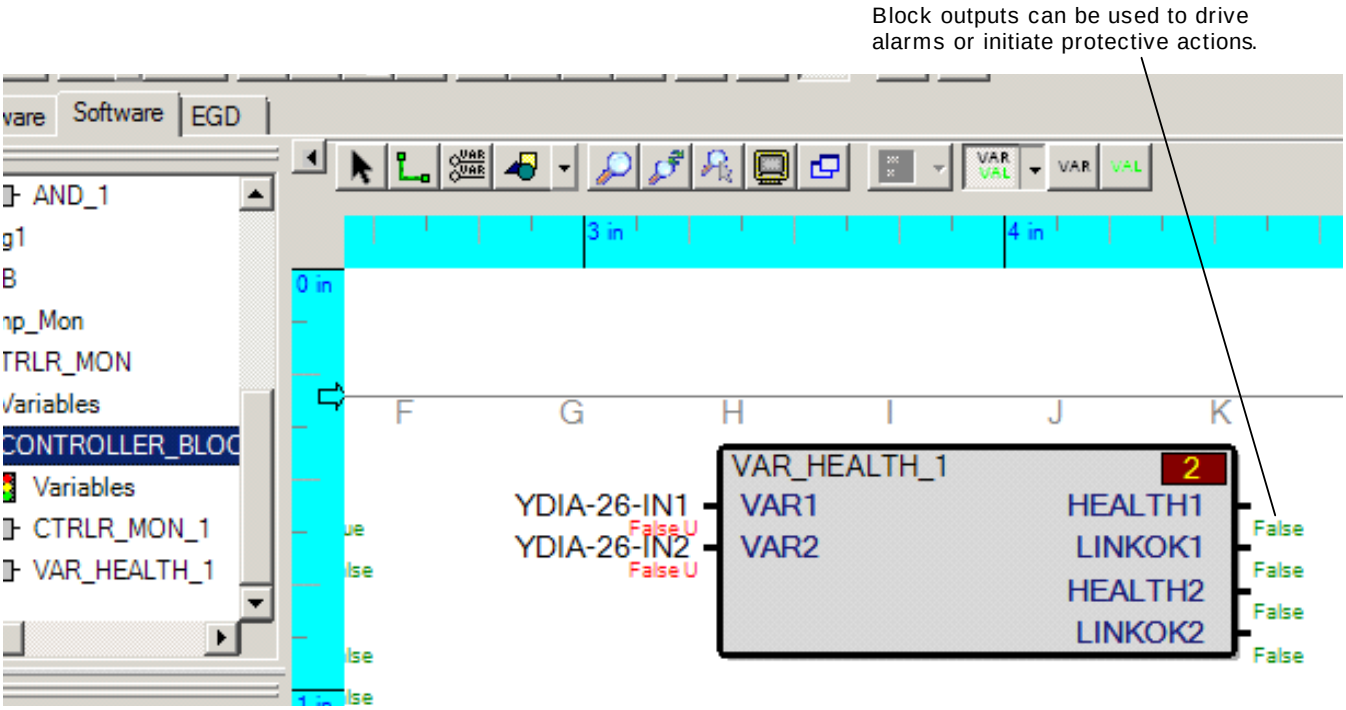
The current value and health of variables connected to YDIA inputs are displayed. **U** indicates an unhealthy value.



From the **PreVote** tab, the T channel is healthy but the R and S channels are not, due to loss of communication.

Variable Health Example

The following ToolboxST screen displays a VAR_HEALTH block. Both variables are connected to the faulted YDOA. Since the cause of the fault is communication, both the HEALTH1 and LINKOK1 output pins are False.



VAR_Health Block Outputs

3.2.1.2 Temperature Monitor

There are two application code blocks available for monitoring the safety controller's temperature: TEMP_STATUS and CTRLR_MON. These controller application code blocks can be used to set alarms, actuate fans, or perform other actions appropriate for the specific environment in which the control cabinet is placed.

3.2.2 Locked Mode

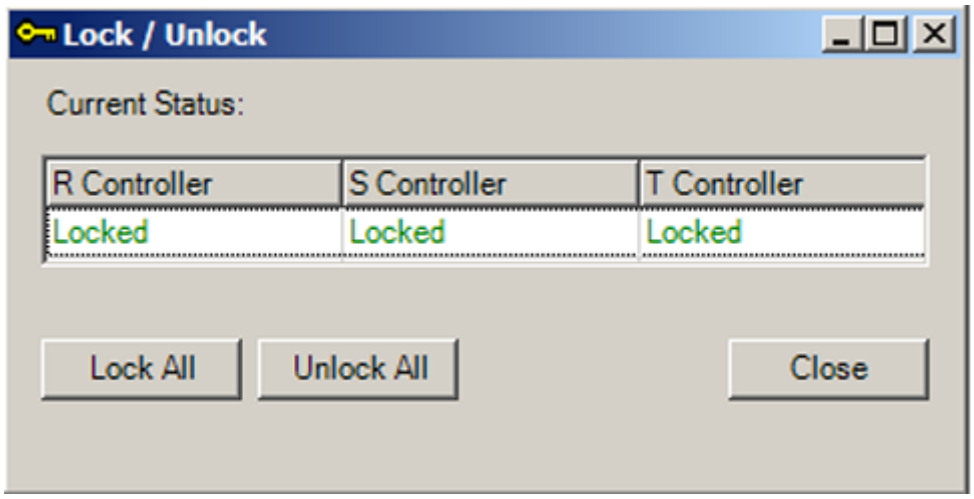
The Mark VIeS Safety control provides a level of protection (LOP) against accidental modification of the safety software through *Locked* mode. In general, all functions or features that have the potential to modify the controller are disabled when in locked mode, for example:

- Variable and constant modification
- Variable forcing
- Application code download
- Firmware download
- Restart commands from ToolboxST application
- External file writes to flash memory
- Low-level diagnostic commands
- Time set commands

The controller starts in *Locked* mode and remains there until an *Unlock* command is received from the ToolboxST application. When the controller receives a *Lock* command from the ToolboxST application or the controller is restarted, it returns to *Locked* mode. When the controller is unlocked, it generates a diagnostic alarm to log the event. The controller tracks its lock state through a configuration variable (for example, *Is_Locked_R*), viewable through the application code, so that appropriate control action can be taken or an external contact can be driven, if desired.

➢ **To lock the controllers**

1. From the Component Editor toolbar, click the key icon. The **Lock / Unlock** dialog box displays.
2. Click the **Lock All** button and the controllers status displays as Locked.



3.2.3 Unlocked Mode

Warning

While in *Unlocked* mode, the Mark VIeS is not inherently less safe than when in *Locked* mode, as SIF implementation is the same. However, when unlocked, the controller could become unsafe, as it is open to modifications that could lead to an unsafe condition.

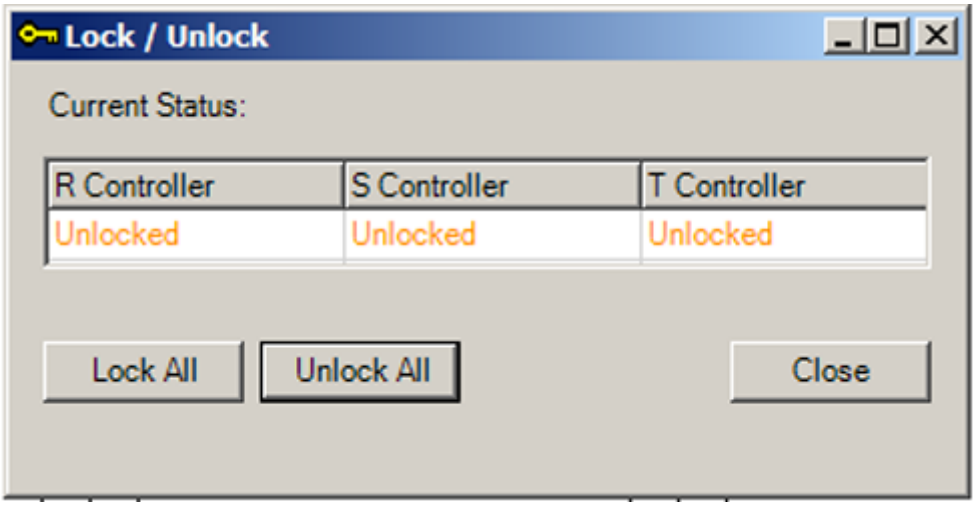
The Mark VIeS allows online application code changes in *Unlocked* mode. Take every precaution to ensure that any online change to application code does not cause an unintended error during the download. This is particularly relevant for dual network configurations in which separate I/O packs are driven by either redundant controller.

The application code does not normally allow safety loops to be activated in *Unlocked* mode. To test a loop in *Unlocked* mode, the permissives preventing operation must be temporarily forced out.

When online repair is required on an operating, redundant system, it is not necessary to unlock the control system to download software. Non-configured I/O packs and controllers boot into Unlocked mode, allowing them to receive the initial software download. The lock status of all the components can be determined by running a download scan.

➢ **To unlock the Mark VIeS Safety controller**

1. From the ToolboxST Component Editor toolbar, click the **Lock/Unlock** (key) icon.
2. From the Lock/Unlock dialog box, click the **Unlock All** button and the controllers status displays as Unlocked.



The Locked state of each controller is displayed at the bottom of the Status tab. If a controller is unlocked and its branded application changed through download, then a diagnostic alarm is generated to announce that the branded application is no longer running. This diagnostic alarm cannot be cleared until the new application is *branded*.

3.2.4 Forced Variables

The controller cannot be locked if any variables are currently forced. All forces must be cleared before issuing a lock command from the ToolboxST application. Forces are not maintained during a startup cycle, so restarting the controller is one method of clearing forces and putting the controller back into the *Locked* mode.

3.2.5 Online Repair

When online repair is required on an operating, redundant system, it is not necessary to unlock the control system to download software. Non-configured I/O packs and controllers boot into Unlocked mode, allowing them to receive the initial software download. The lock status of all the components can be determined by running a download scan.

3.2.6 Branding

Application code and configuration that is part of a SIF must be certified per *IEC 61511* prior to use. To facilitate this activity, the controller allows the user to designate a particular set of code as acceptable for its intended purpose. In the ToolboxST application, this process is called *branding*. Branding is also required after upgrades from BPPB to BPPC based Safety I/O packs.

When the code is branded, the controller calculates a checksum of all application code and configuration information, and retains it in nonvolatile memory. Whenever the application code or I/O pack configuration is modified, the controller detects the difference and generates a diagnostic alarm. Similarly, until the application code has been initially branded, a diagnostic alarm will be active noting the fact.

The current cyclic redundancy check (CRC) values are displayed by the ToolboxST application and available to the application code (such as *CurrentAppCrc_R*). If any I/O pack faults or is turned off, the controllers interpret this as a CRC difference and the diagnostic alarm is generated.

A yellow **Not Equal** indicates that changes to the application code have not yet been downloaded to the controller.

A green brand indicated that a controller is executing branded application code. Matching brands between redundant controllers show that all controllers are running the same application code.

Log | Status | History | Where Used | Find Results | Info

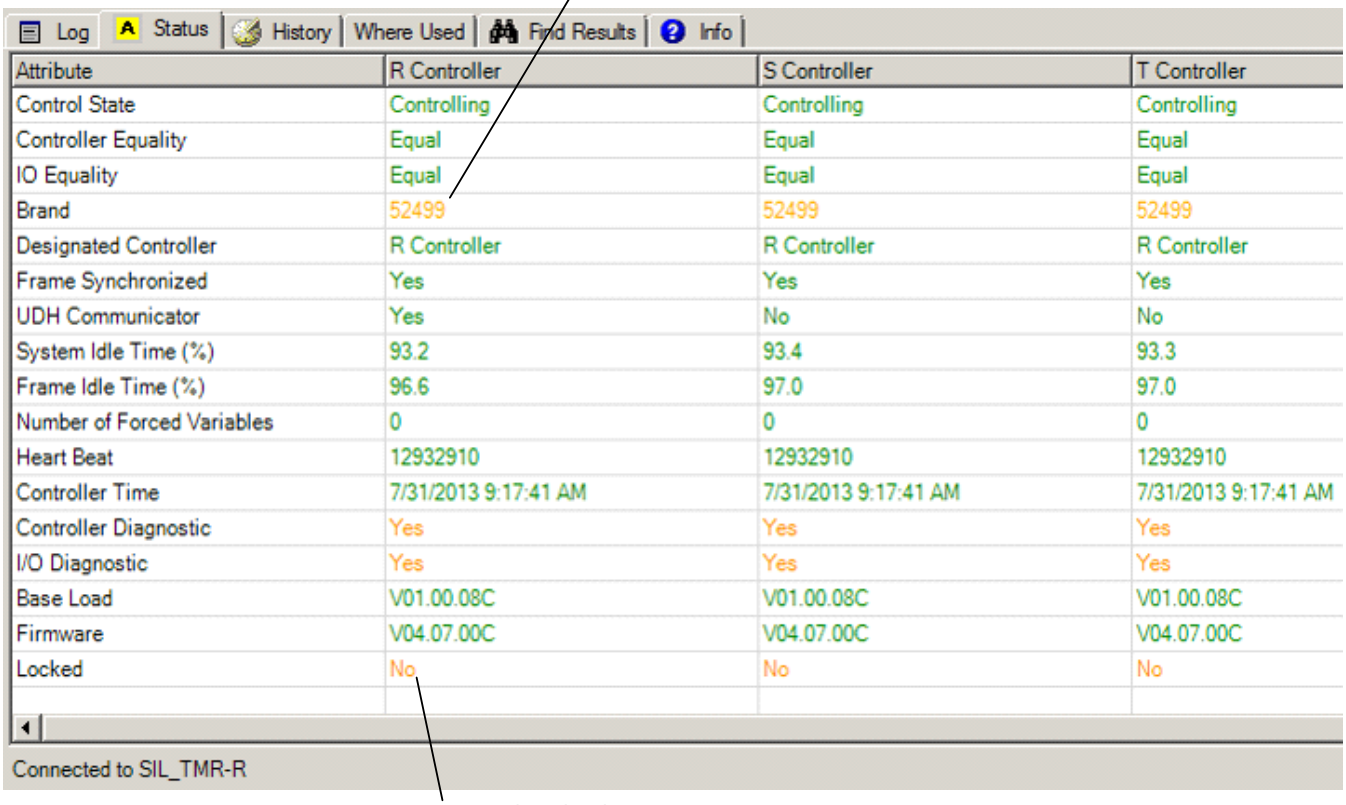
Attribute	R Controller	S Controller	T Controller
Control State	Controlling	Controlling	Controlling
Controller Equality	Not Equal	Not Equal	Not Equal
IO Equality	Equal	Equal	Equal
Brand	59317	59317	59317
Designated Controller	R Controller	R Controller	R Controller
Frame Synchronized	Yes	Yes	Yes
UDH Communicator	Yes	No	No
System Idle Time (%)	93.2	93.3	93.4
Frame Idle Time (%)	96.5	97.0	96.9
Number of Forced Variables	0	0	0
Heart Beat	12927990	12927990	12927990
Controller Time	7/31/2013 9:14:24 AM	7/31/2013 9:14:24 AM	7/31/2013 9:14:24 AM
Controller Diagnostic	Yes	Yes	Yes
I/O Diagnostic	Yes	Yes	Yes
Base Load	V01.00.08C	V01.00.08C	V01.00.08C
Firmware	V04.07.00C	V04.07.00C	V04.07.00C
Locked	No	No	No

Connected to SIL_TMR-R

Before Download

After download but before branding, the following Status displays.

A yellow brand indicates that the application currently running in the controller does not match the previous brand and needs to be certified and branded prior to use in a SIF.



Note To download an application code change, the controllers must be unlocked.

➢ **To brand the controller's application and configuration:** from the ToolboxST **Component Editor** toolbar, click the **Brand** icon**.**

After branding, the text turns green and all three controllers match. The controllers are also *locked* to prevent further changes.

Log | Status | History | Where Used | Find Results | Info

Attribute	R Controller	S Controller	T Controller
Control State	Controlling	Controlling	Controlling
Controller Equality	Equal	Equal	Equal
IO Equality	Equal	Equal	Equal
Brand	52499	52499	52499
Designated Controller	R Controller	R Controller	R Controller
Frame Synchronized	Yes	Yes	Yes
UDH Communicator	Yes	No	No
System Idle Time (%)	92.9	93.0	93.2
Frame Idle Time (%)	96.6	97.0	96.9
Number of Forced Variables	0	0	0
Heart Beat	12934377	12934377	12934377
Controller Time	7/31/2013 9:18:40 AM	7/31/2013 9:18:40 AM	7/31/2013 9:18:40 AM
Controller Diagnostic	Yes	Yes	Yes
I/O Diagnostic	Yes	Yes	Yes
Base Load	V01.00.08C	V01.00.08C	V01.00.08C
Firmware	V04.07.00C	V04.07.00C	V04.07.00C
Locked	Yes	Yes	Yes

Connected to SIL_TMR-R

Branded and Locked

3.2.7 Startup Shutdown Process

The safety control system can shut down either by manual operator action or automatically as a result of certain detected fault conditions. A number of protective features are included in the Mark VIeS Safety control to ensure that a SIF is not compromised by inadvertent modifications made to the system. These features include an operating *Locked* mode, which prevents unwanted changes, and application code branding, which detects configuration changes.

3.2.7.1 Manual Shutdown

A manual shutdown occurs when the controller power supply is manually turned off. When power is reapplied, the controller proceeds through control startup states that are designed to synchronize its application states with the other redundant controllers. Forced values are not retained through a power down cycle. If forced values exist and only one controller of a redundant set is restarted, forcing will be restored and the restarted controller will obtain those forced values from the designated controller during the Data Initialization control state. The restarted controller enters the same locked state as the designated controller.

3.2.7.2 Fault Detected Shutdown

When fault conditions are detected, the Mark VIeS controller either restarts or enters a fail-safe control state, depending on the type of fault condition. In the event of a processor restart, the I/O packs are programmed to operate in their fail-safe state.

The controller restarts on three conditions:

- Software watchdog timeout
- Hardware watchdog timeout
- Operating system process control failure

The watchdog timer functions are generally meant to ensure safe controller operation in conditions where one or more runtime processes are overloaded. Each periodic safety-critical process initializes and then continually tickles one or more software watchdog timers, which are implemented by the system firmware process and configured with expected tickle rates. If a watchdog timer is tickled too quickly, too slowly, or not at all, the system process restarts the controller.

When using a hardware watchdog timer, a backup watchdog process is also implemented. If this process fails to tickle the hardware watchdog timer quickly enough, the board restarts.

In addition to watchdog timeouts, a process control failure in the operating system can cause an automatic restart. If any runtime process, other than the system process, fails to run due to a problem, the operating system prompts the system process to restart the controller. If the system process fails, the hardware watchdog process detects the failure of the software watchdog function and forces a restart by not tickling the hardware watchdog timer.

A different set of fault conditions cause the controller to enter its fail-safe control state, instead of restarting the controller. In this state, the controller outputs to the I/O packs are disabled, forcing the I/O packs, in turn, to enter their fail-safe state. In this state, I/O packs drive their physical outputs to safe values as configured.

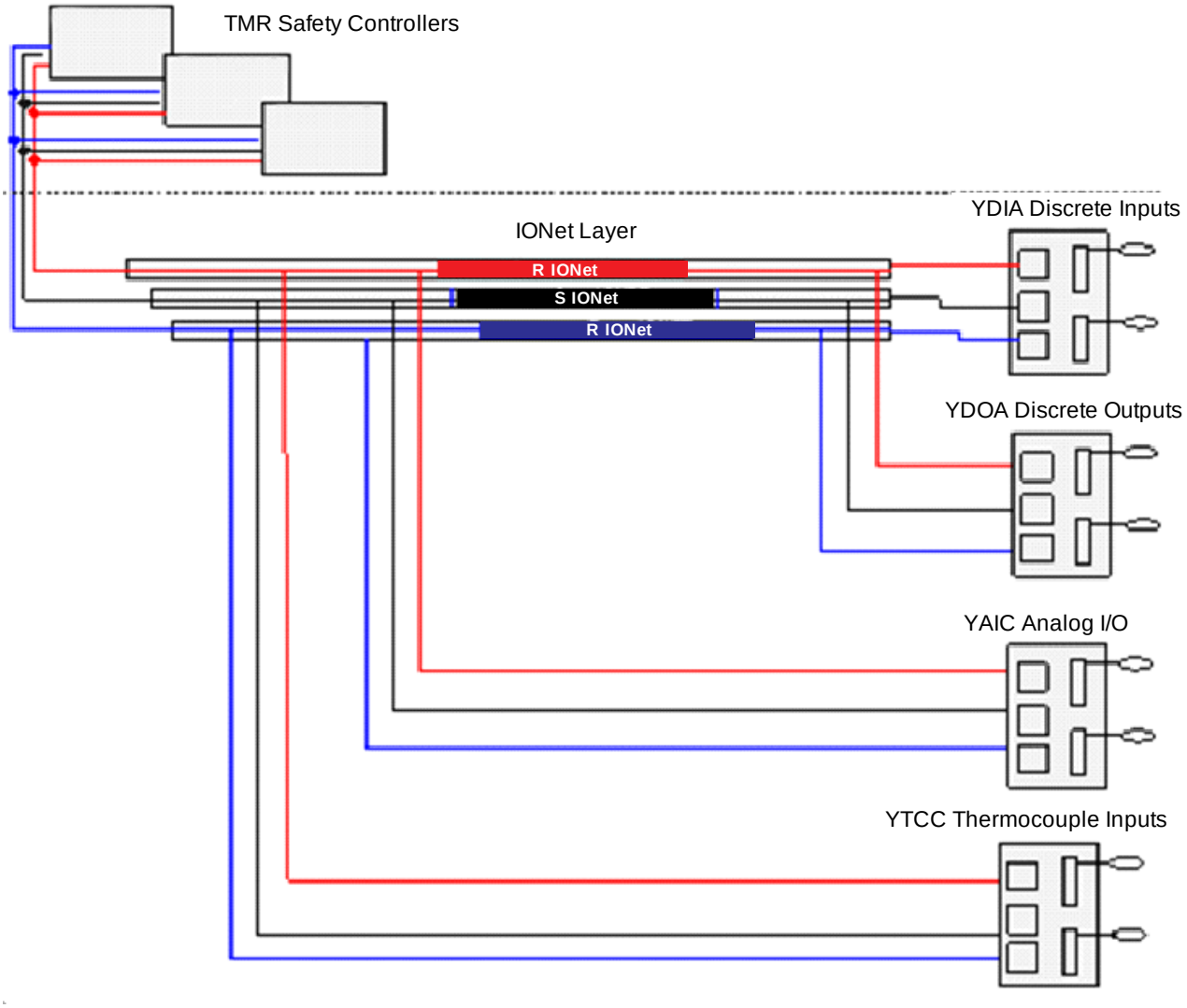
In the controller, the sequencer process continuously conducts the following program flow integrity malfunction tests:

- Critical process order of execution
- Critical process scheduling overrun and under-run
- Frame period
- Frame state timeout intervals
- Frame number

If any of these tests fail three consecutive times (generally three frames), appropriate diagnostic alarms are generated. After five successive failures, the system is placed in the fail-safe control state.

3.3 Online SIFs

The Mark VIeS control components used by the online SIFs and their interconnections in TMR architecture are displayed in the following figure.



Controller and I/O – TMR Control Mode

The figure also illustrates the top-level architecture for SIL 3 capability, using a TMR, 2 out of 3, safety architecture. This deployment architecture is referred to in Mark VIeS documentation as the TMR Control Mode.

3.4 Redundancy

The Mark VIeS Safety control can be set up in various traditional safety architectures that allow selections among SIL capability, availability, and cost to better serve the specific needs of an application. TMR, dual, and simplex control modes are supported.

The controllers are designated as R, S, and T in a TMR system, R and S in a dual system, and R in a simplex system. Each controller owns one IONet. The R controller sends outputs to an I/O module through the R IONet, the S controller sends outputs through the S IONet, and the T controller sends outputs through the T IONet.

IONet features include:

- Ethernet User Datagram Protocol (UDP) using Dynamic Host Configuration Protocol (DHCP) for network address assignments. While based on Ethernet hardware and protocol standards, the IONet is maintained as a separate physical network to avoid risks of interference from other network traffic.
- Full duplex Ethernet switches throughout, so no message collisions impact system timing
- IEEE® 1588 protocol through the R, S, and T IONets to synchronize the clock of the I/O modules and controllers to within ±100 microseconds
- Coordination of IONet traffic and controller action to ensure minimum predictable latency for inputs (given IEEE 1588 timing alignment). Controller outputs take place at the same time and all output I/O packs exhibit consistent latency in processing and updating the outputs.

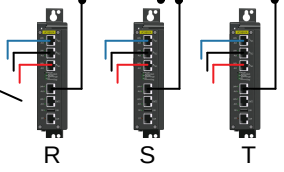
3.4.1 TMR Control Mode

In the TMR control mode, three independent controllers communicate with the I/O through three independent IONet channels. The TMR control mode with a hardware fault tolerance (HFT) of 1 is designed for SIL 3 capability with the running reliability of 2 out of 3 redundancy. Each independent controller receives three independent sets of input data, one from each IONet for 2 out of 3 input voting. Controller outputs are 2 out of 3 voted in the output circuitry. TMR control mode functions are as follows:

- TMR (2 out of 3): SIL 3 high and low demand for de-energize-to-trip applications
- TMR (2 out of 3): SIL 2 low demand for energize-to-trip applications
- TMR (2 out of 3): SIL 2 high and low demand vibration (YVIBS1A) applications
- Degraded TMR (1 out of 2): SIL 3 high and low demand for de-energize-to-trip applications
- TMR degradation sequence: (2 out of 3) → (1 out of 2) → Fail Safe

TMR Controllers
Three Mark VIeS controllers work as a set synchronizing data every frame (sweep). Each controller receives inputs on all 3 I/O networks, and sends output commands on designated I/O network.

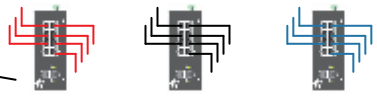
PC Based Gateway
PC based communication interface, options:
- OPC-DA server
- OPC-UA server
- Modbus master

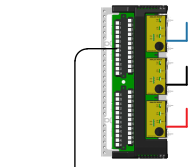


Third Party Control System

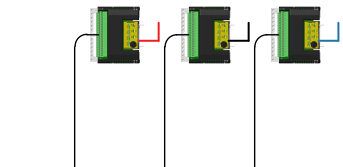
Embedded Controller Gateway
Embedded controller for communication interface, options:
- OPC-UA server
- Modbus slave

TMR I/O Network
Ethernet based TMR I/O network supports both centralized and distributed I/O modules.

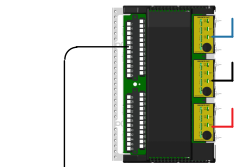




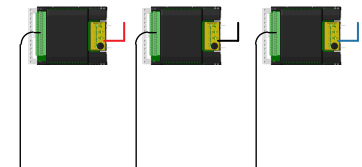
TMR Fanned Input
Single discrete/ analog sensor is fanned through a common terminal board to three independent input packs, 2oo3 voting is done in the controller set.



TMR Dedicated Input
Three redundant discrete/analog sensors are wired to three independent input modules, 2oo3 voting is done in the controller set.



TMR Outputs Voted on Terminal Board
The three packs receive output commands from their associated controller, the common terminal board then performs 2oo3 voting on the outputs and controls the discrete actuator.

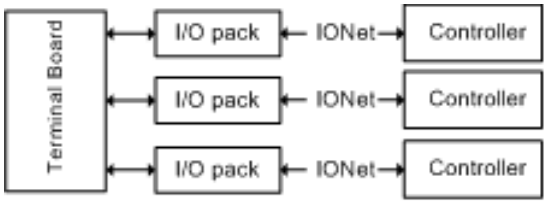


TMR Outputs Voted in Actuator
Three independent output modules receive the output command from their associated controller, then command the actuator, 2oo3 voting performed in the actuator.

When TMR controllers are present in a system, dual and simplex inputs and simplex outputs, in addition to TMR I/O pack, can be used. This allows for a mix of redundancy within a single system. Some I/O packs can be TMR to support SIL 3 for critical safety functions, while other I/O packs can use less hardware and support a lower SIL for less critical functions.

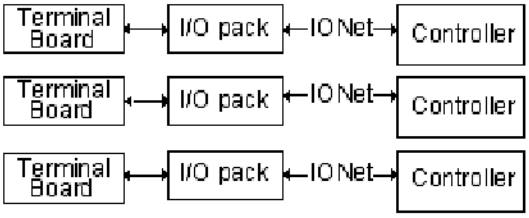
TMR redundancy for I/O packs can be either dedicated (each mounted to individual S-type terminal boards) or TMR fanned (each mounted to a single T-type terminal board). With TMR, each I/O pack for field input and output is uniquely associated with only one IONet.

With TMR fanned I/O, each input point is read by three independent I/O packs that receive the actual field input through a common terminal board that fans the input to each of the three I/O packs. Each I/O pack receives output messages from its own controller. The three independent I/O pack outputs are then 2 out of 3 hardware voted on a common terminal board.



TMR Fanned Mode with Three I/O Packs and One T-type Terminal Board

With TMR dedicated, the outputs or inputs for each I/O pack can be connected to an independent terminal board, allowing the 2 out of 3 voting to be performed in the field output devices outside the Mark VIeS control.



Dedicated Mode with Three I/O Packs and three S-type Terminal Boards

3.4.2 Dual Control Mode

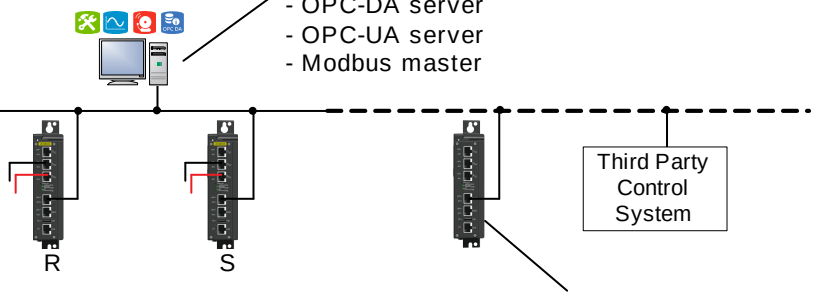
The dual control mode contains two controllers, two IONets, and either a single I/O pack or fanned TMR I/O packs. In a dual system, the level of I/O reliability can be varied to meet the application needs for specific I/O packs.

Dual control mode functions are as follows:

- Dual (1 out of 2): SIL 3 high and low demand for de-energize-to-trip applications.
- Dual (1 out of 2): SIL 2 high and low demand vibration (YVIBS1A) applications
- Dual (2 out of 2): SIL 2 low demand for energize and de-energize-to-trip applications
- Dual (2 out of 2): SIL 1 low demand vibration (YVIBS1A) applications

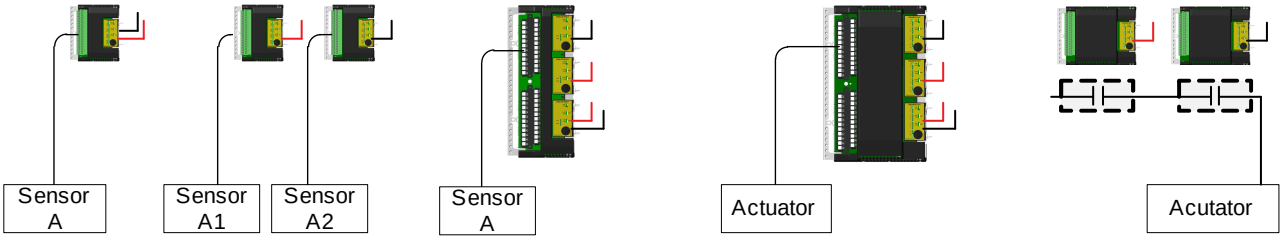
Dual Controllers
Dual Mark VIeS controllers work as a controller set synchronizing data every frame (sweep). Each controller receives inputs on both I/O networks, and sends output commands on designated I/O network.

PC Based Gateway
PC based communication interface, options:
- OPC-DA server
- OPC-UA server
- Modbus master



Dual I/O Network
Ethernet based dual I/O network supports both centralized and distributed I/O modules.

Embedded Controller Gateway
Embedded controller for communication interface, options:
- OPC-UA server
- Modbus slave



Single Sensor
Single sensor wired to a single input module with dual I/O network to controller set.

Dual Sensor
Dual sensors wired to independent input modules with independent I/O networks to controller set.

TMR Fanned Input
Single sensor is fanned through a common terminal board to three independent input packs, 2oo3 voting done in the controller set.

TMR Outputs Voted on Terminal Board
The three output packs receive an output command from designated controller, the common terminal board then performs 2oo3 voting and controls the actuator.

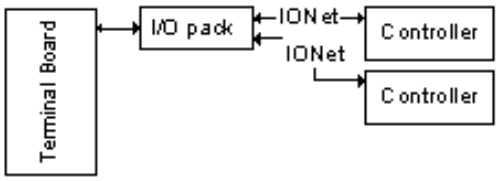
1oo2 De-energize to Trip in Output Modules
Two independent output modules receive the output command from designated controller, combination of two creates 1oo2 de-energize to trip function across the two modules.

In a dual Mark VIeS Safety control, both controllers receive inputs from the I/O packs on both networks and continuously transmit outputs on their respective IONet. Since redundant data is transmitted continuously from the I/O pack and controller, both the pack and controller must select which network to use.

At power up, the controller or I/O pack listens for data on both networks. The channel that delivers the first valid packet becomes the preferred network. The I/O pack or controller uses this data as long as the data continues to arrive on that channel. If the preferred channel does not deliver the data in a frame, the other channel becomes the preferred channel if it supplies valid data. This prevents a given I/O pack/controller from bouncing back and forth between two sources of data. As a result, different I/O packs/controllers may have separate preferred data sources, but this can also happen if a component fails.

3.4.2.1 Single I/O Pack Dual Network I/O Module

The I/O option A is a single I/O pack dual network I/O module setup. This configuration is typically used for single sensor I/O. A single sensor connects to a single set of acquisition electronics but connects to two networks.



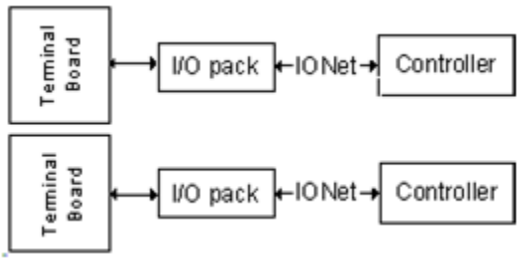
Dual Mode with One I/O Pack and Two IONets

The I/O pack delivers input data on both networks at the beginning of the frame and receives output data from both controllers at the end of the frame. The reliability and availability features include:

- HFT 0
- Single data acquisition
- Redundant network

3.4.2.2 Dual Single I/O Pack Single Network I/O Module

The I/O option B is two single pack, single network I/O modules. This configuration is typically used for inputs that have multiple sensors monitoring the same process points. Two sensors are connected to two independent I/O modules.



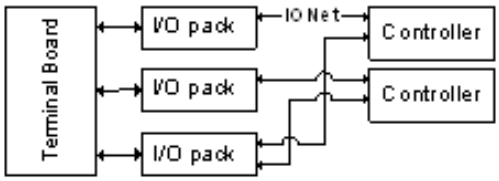
Dual Mode with Two Single Pack, Single IONet Modules

Each I/O pack delivers input data on a separate network at the beginning of the frame and receives output data from separate controllers at the end of the frame. The reliability and availability features include:

- HFT 1
- Redundant sensors
- Redundant data acquisition
- Redundant network
- Online repair

3.4.2.3 Triple I/O Pack Dual Network I/O Module

The I/O option C is a special case mainly intended for outputs but can also apply to inputs. The special output voting/driving features of the TMR I/O modules can be used in a dual control system. The inputs from these modules are selected in the controller.



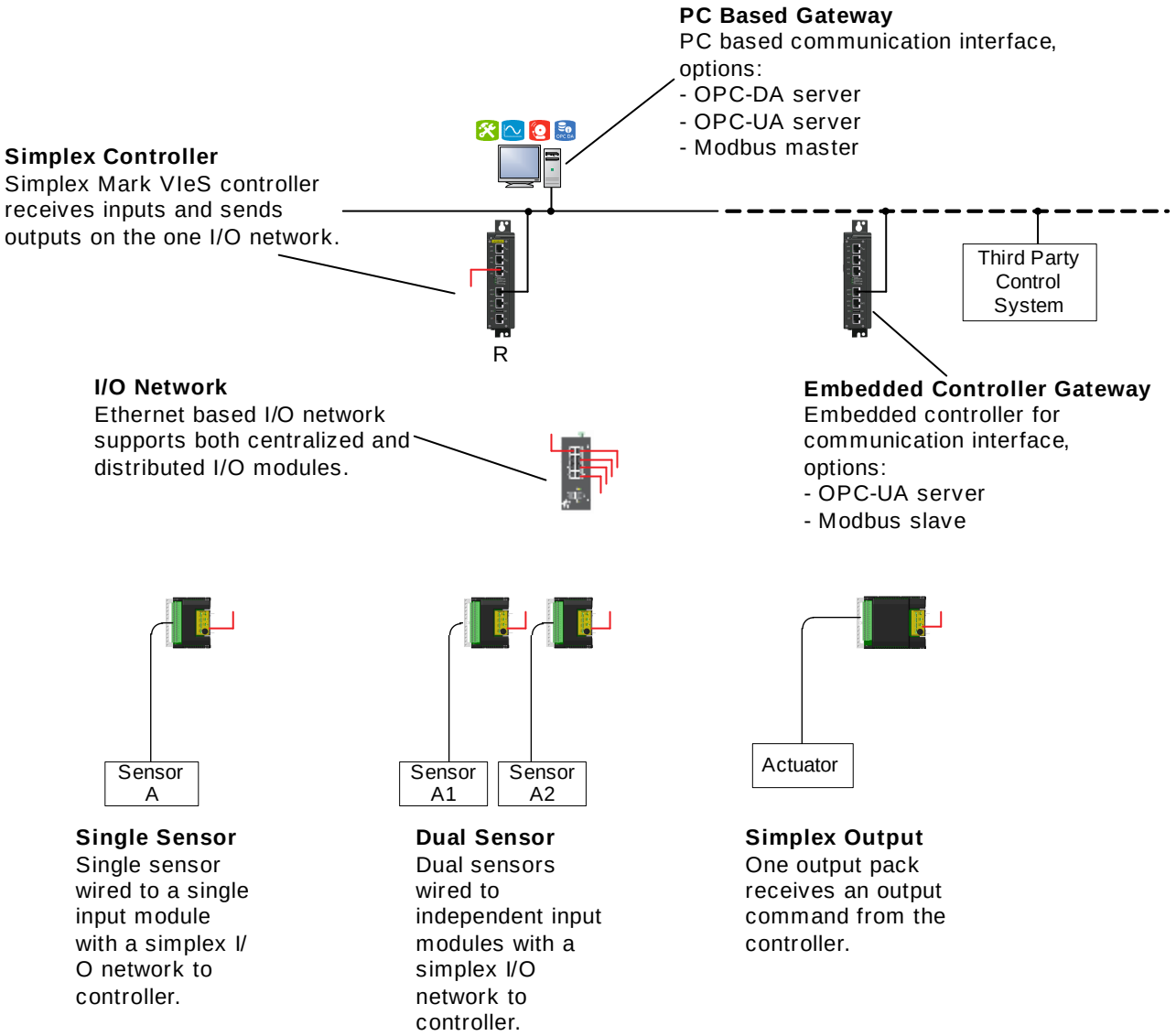
Dual Mode with Three I/O Packs and Two Simplex and One Duplex IONet

Two I/O packs connect to separate networks to deliver input data and receive output data from separate controllers. The third I/O pack is connected to both networks. This I/O pack delivers inputs on both networks and receives outputs from both controllers. The reliability and availability features include:

- HFT 1
- Redundant data acquisition
- Output voting in hardware
- Redundant network
- Online repair

3.4.3 Simplex Control Mode, 1 out of 1

Simplex (1 out of 1) control mode is SIL 2 low demand capable for de-energize-to-trip and SIL 1 for vibration applications. Each I/O pack delivers an input packet at the beginning of the frame on its primary network. The controller sees the inputs from all I/O packs, runs application code, and delivers a broadcast output packet(s) that contains the outputs for all I/O modules.



3.5 Control and Protection

3.5.1 Output Processing

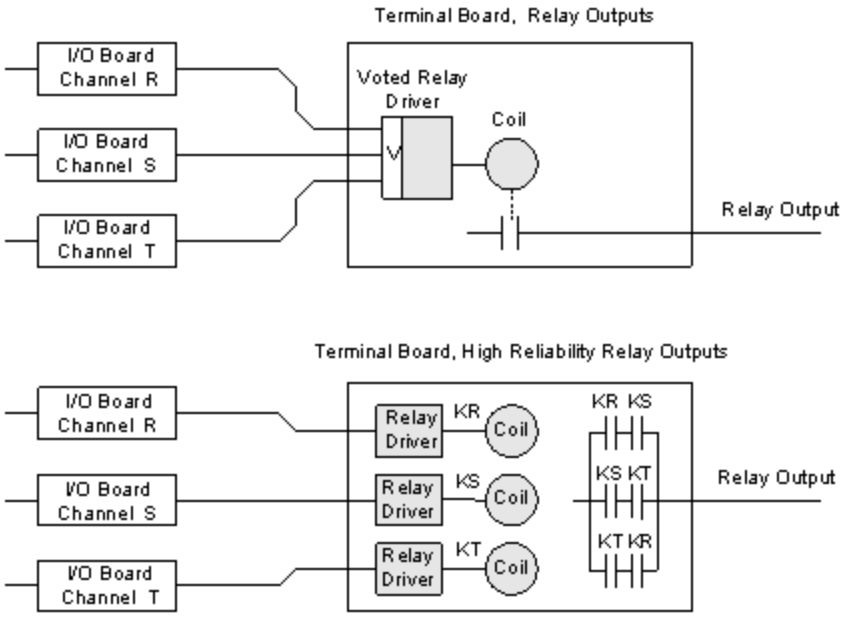
The system outputs must be transferred to the external hardware interfaces and then to the various actuators controlling the process. TMR outputs are voted in the output voting hardware, and any system can also output individual signals through simplex hardware.

The three voting controllers calculate TMR system outputs independently. Each controller sends the output to its associated I/O hardware (for example, R controller sends to R IONet). A voting mechanism then combines the three independent outputs into a single output. Different signal types require different methods of establishing the voted value.

The signal outputs from the three controllers fall into three groups:

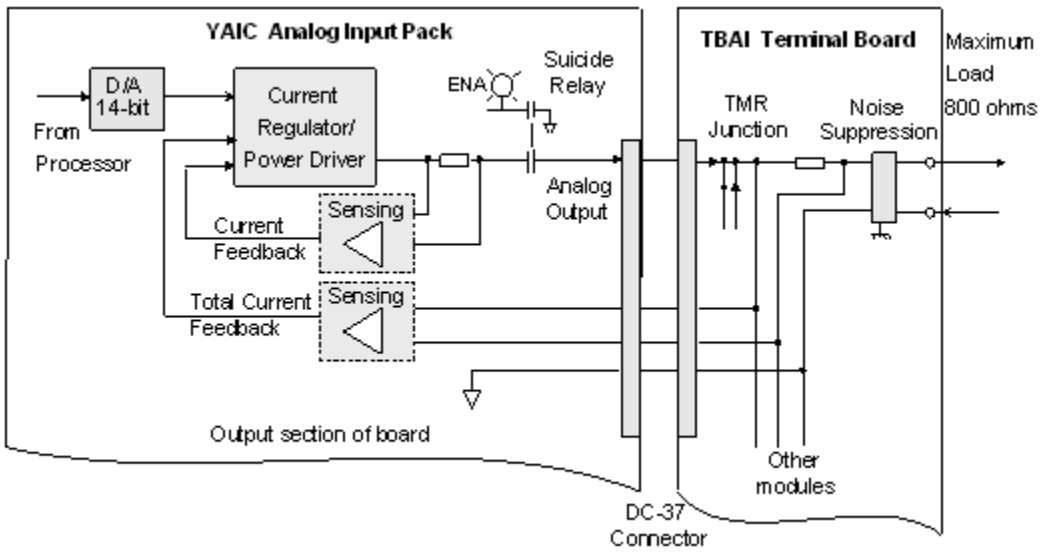
- Outputs driven as single-ended non-redundant outputs from individual IONets
- Outputs on all three IONets that are merged into a single signal by the output hardware
- Outputs on all three IONets that are output separately to the controlled process. This process may contain external voting hardware.

For normal relay outputs, the three signals feed a voting relay driver, which operates a single relay per signal. For more critical protective signals, the three signals drive three independent relays with the relay contacts connected in the typical six-contact voting configuration.



Relay Outputs for Protection

The following figure displays 4-20 mA signals combined through a 2 out of 3 current sharing circuit that votes the three signals to one. This unique circuit ensures the total output current is the voted value of the three currents. When the failure of a 4-20 mA output is sensed, a deactivating relay contact is opened.



TMR Circuit for Voted 4-20 mA Outputs

3.5.1.1 I/O Pack Communication Loss

Each I/O pack monitors the IONet for valid commands from one or two controllers. If a valid command is not received within an expected time, the I/O pack declares communication as lost. Upon loss of communication, the I/O pack action is configurable as follows:

- The default action is the power-down state, as if the power were removed from the I/O pack
- Continue to hold the last commanded value indefinitely
- Commanded to go to a specified output state

Caution

For critical loops, the default action is the only acceptable choice because it is the assigned behavior for I/O pack failure on power loss failure. The other options are provided for non-critical loops in which running reliability may be enhanced by an alternate output.

3.5.2 Input Processing

All inputs are available to all three controllers and input data is handled in several ways. For those input signals that exist in only one I/O module, all three controllers use the same value as a common input without voting. Signals that appear in all three I/O channels are voted to create a single input value. The triple inputs can come from independent sensors or from a single sensor by hardware fanning at the terminal board.

I/O Configurations

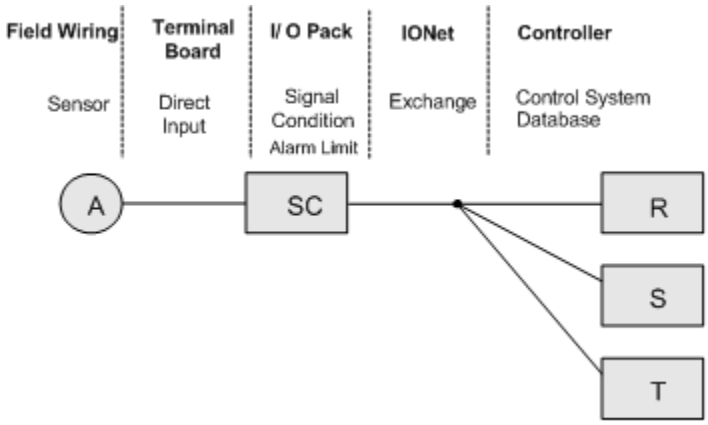
I/O	Topology	TMR	Dual	Simplex
Simplex	1 pack, 1 IONet*	X	X	X
Dual	1 pack, 2 IONets 2 packs, 1 IONet 3 packs, 1/1/2 IONet	X X N/A	X X X	
TMR	Fanned – 3 packs, 1 IONet/pack Dedicated – 3 packs, IONet/pack	X X		
* The number of IONets in a system must equal the number of controllers.				

For any of the input configurations, multiple inputs can be used to provide application redundancy. For example, three simplex inputs can be used and selected in application code to provide sensor redundancy.

The Mark VIeS control provides configuration capability for input selection and voting using a simple, reliable, and efficient selection/voting/fault detection algorithm. This reduces application configuration effort, maximizing the reliability options of a given set of inputs and providing output voting hardware compatibility. For a given controller topology, terminal board redundancy ≤ the controller topology is available. For example, in a TMR controller, all simplex and dual option capability is also provided.

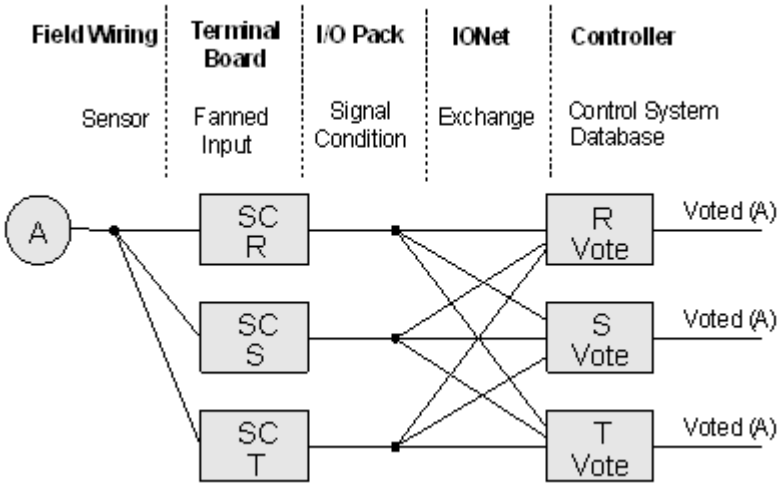
While each IONet is associated with a specific controller, all controllers see all IONets. The result is that for a simplex input, the data is seen not only by the output owner of the IONet, but also by any other controllers in parallel. The benefit is that the loss of a controller associated with a simplex input does NOT result in the loss of that data. The simplex data continues to arrive at other controllers in the system.

A single input can be brought to the three controllers without any voting as indicated in the following figure. This is used for generic I/O, such as monitoring 4-20 mA inputs, contacts, and thermocouples.



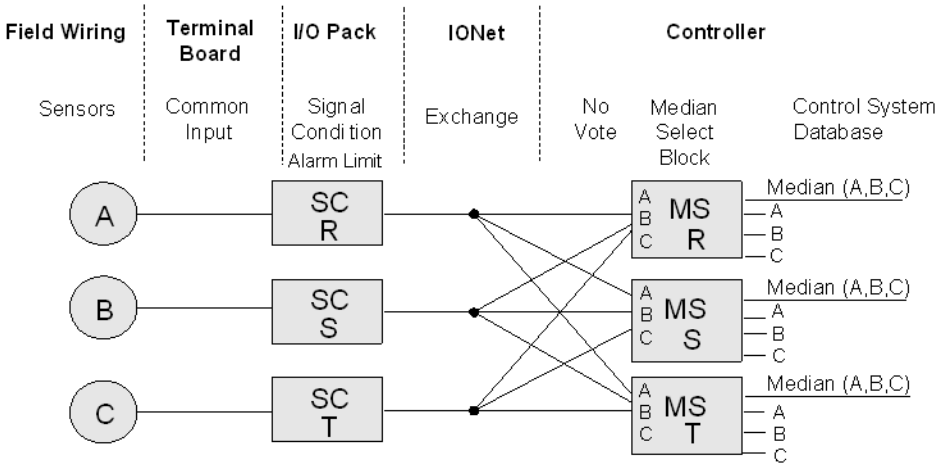
Single Input without Software Voting

For medium integrity applications with medium to high reliability sensors, one sensor can be fanned to three I/O boards as shown in the following figure. Three such circuits are needed for three sensors. Typical inputs include 4-20 mA inputs, contacts, and thermocouples.



One Sensor with Fanned Input and Software Voting

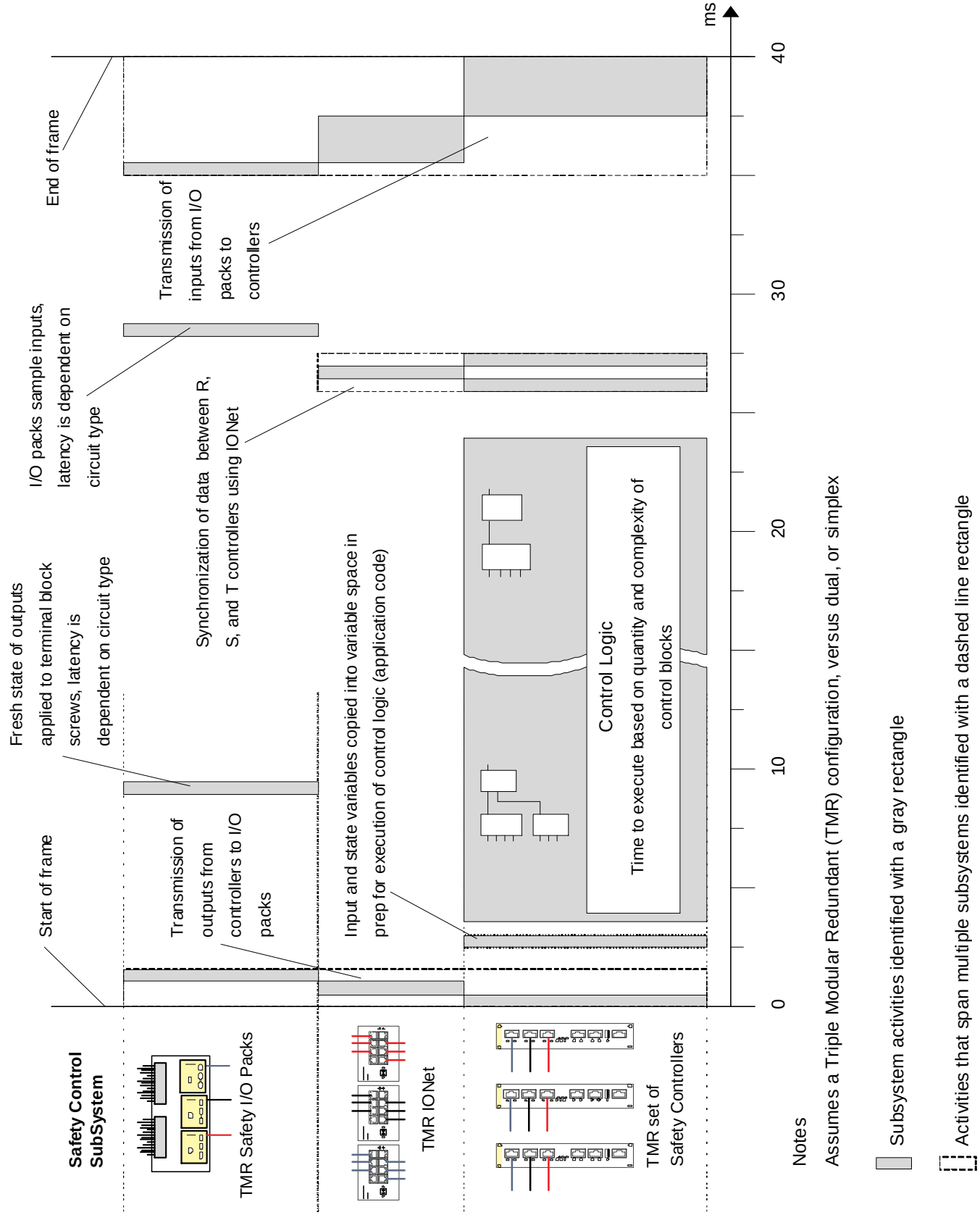
Three independent sensor inputs can be brought into the controllers without voting to provide the individual sensor values to the application. Median values can be selected in the controller if required. This configuration, displayed in the following figure, is used for special applications only.



Three Independent Sensors with Common Input, Not Voted

3.6 Critical System Timing Parameters

Critical System Timing Parameters control is a discrete time, sampled system. The fundamental frame rate or scan period of the controller is selectable by the user (10 ms, 40 ms, 80 ms, or 160 ms) and should be related to the required process safety time for the fastest SIF in the system. The following figure provides a typical sequence of events within the scan frame (40 ms is shown in this example).


Safety Control SubSystem
TMR Safety I/O Packs
TMR IONet
TMR set of Safety Controllers
Start of frame
Transmission of outputs from controllers to I/O packs
Fresh state of outputs applied to terminal block screws, latency is dependent on circuit type
Input and state variables copied into variable space in prep for execution of control logic (application code)
Synchronization of data between R, S, and T controllers using IONet
I/O packs sample inputs, latency is dependent on circuit type
Transmission of inputs from I/O packs to controllers
End of frame
Control Logic
Time to execute based on quantity and complexity of control blocks
0
10
20
30
40
ms
Notes
Assumes a Triple Modular Redundant (TMR) configuration, versus dual, or simplex
Subsystem activities identified with a gray rectangle
Activities that span multiple subsystems identified with a dashed line rectangle

3.6.1 Maximum Remote I/O Stimulus to Response Time

The Mark VIeS Safety control and I/O has a worst case response time of < 300 ms. It is suitable for use in a SIF with a process safety time (PST) of 500 ms or higher and does not consume more than 60% of this budget. The individual components of the timing analysis are as follows:

- If input changes directly after last input sample, the worst case delay on the sample is one frame period (10, 40, 80 or 160 ms)
- Input sample to transmit over IONet is < 5 ms
- Controller receives inputs, runs programs, and sends outputs in < one frame period (10, 40, 80 or 160 ms)
- Output receives updated outputs and sets physical outputs in < 5 ms
- Physical output relays have a worst case 40 ms response.
- Total worst case time without any lost IONet communication is 2 x frame period + 50 ms (for input or output transfer).
- Worst case additional communication delay due to lost message without timeout is 3 x frame period up and 1 x frame period down, or 4 x frame period total.
- Total worse case response without timeout† (including lost IONet communications) is 6 x frame period + 50 ms.
  - Assumes a frame period of either 10, 40, 80 or 160 ms
  - Assumes maximum number of messages missed in both directions
  - Assumes initial stimulus slightly missed previous input sample time
  - Assumes common cause across IONets

Note † Timing assumes use of fastest input I/O pack filter settings. This is the sum of total worst case time without any lost IONet communication and worst case additional communications delay due to lost message without timeout.

Maximum Local I/O Stimulus to Response Time

The Mark VIeS Safety control turbine-specific I/O can supply high-speed I/O for turbine protection functions with a worst case response time of < 60 ms. It is suitable for use in a SIF with a PST of 100 ms or higher, and does not consume more than 60% of the budget. The individual components of the timing analysis are as follows:

- Local I/O timing is independent of redundancy architecture
- Local I/O operates at 10 ms frame rate
- If input changes directly after last input sample, the worst case delay on the sample is 10 ms
- Input change to be seen by I/O processor board is < 5 ms
- Local control algorithm receives inputs, runs user programs, and sends outputs in 10 ms
- Physical output relays have a worst case 40 ms response
- Total worst case time 55 ms (for input or output transfer)

Note If TRPA or TREA with solid-state relays are used, relay response is < 1 ms. This reduces local response time to < 20 ms.

3.6.2 Diagnostic Interval

All system self-diagnostics are conducted within a one-hour interval.

3.6.3 Mark VIeS Safety Controller Response to Loss of Communication

3.6.3.1 Single Network I/O Pack Input

When communication between a controller and a one-network I/O pack fails, in the first frame the signal health is declared bad and the input variable is maintained at the last value received. During the third frame an alarm is generated. During the fifth frame the signal value is set to the default value.

Single Network I/O Pack Input Response to Loss of Input

Input Variables	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last				Default

3.6.3.2 Dual Network or Dual One-Network I/O Pack Input

Upon failure of IONet communication with a single input, dual network I/O pack or a dual input, one-network I/O pack, the controller responds as follows. During the first frame after loss, the controller declares the buffer health bad, drives the input variable by the remaining valid network input, and holds the signal as healthy. During the third frame, an alarm is generated and, during the fifth frame, the input buffer value is set to the default value.

Dual Network I/O Pack Input Response to Loss of First Input

Input Buffer	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last				Default
Input Variables					
Health	Healthy				
Values	2nd input				

When the second input is lost, the input variable health immediately goes bad and the value is held at the most recent value received. In the third frame, an alarm is generated. During the fifth frame, the input variable is set to the default value.

Dual Network I/O Pack Input Response to Loss of Second Input

Input Buffer	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last				Default
Input Variables					
Health	Unhealthy				
Values	Hold last				Default

3.6.3.3 Triple Redundant I/O Pack Input

The controller response to the loss of triple redundant input signals depends on the number of lost inputs. Upon loss of the first input signal, the prevote buffer for the lost signal is identified as unhealthy, held at the previous value for one frame, and set to the default value during successive frames. During the third frame, an alarm is generated, the input variable health remains good (HFT of 1), and the voted variable remains valid.

Controller Response to Loss of First Input

Prevote Buffer	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last	Default			
Input Variables					
Health	Healthy				
Values	Voted				

Upon loss of the second input, the input variable health is immediately set unhealthy and, for one frame, the prevote buffer is held at the most recent value. During the second frame, the input variable value is set to the default value. An alarm is generated during the third frame.

Controller Response to Loss of Second Input

Prevote Buffer	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last	Default			
Input Variables					
Health	Unhealthy				
Values	Voted	Default (from vote)			

Upon loss of the third input, the input variable health is immediately set unhealthy and, for one frame, the prevote buffer is held at the most recent value. During the first frame, the input variable value is set to the default value. An alarm is generated during the third frame.

Controller Response to Loss of Third Input

Prevote Buffer	Frame 1	Frame 2	Frame 3	Frame 4	Frame 5
Health	Unhealthy				
Alarm			Send		
Values	Hold last	Default			
Input Variables					
Health	Unhealthy				
Values	Default (from vote)				

3.6.4 I/O Pack Response to Loss of Communication

3.6.4.1 Single Network I/O Pack Output

When an output pack does not receive communications from the controller, it holds the last value for one frame, goes to the defined condition in the second frame, and generates an alarm in the third frame. The defined output condition defaults to the power-down state and should be used in most safety systems. Options are provided so that the I/O pack continues to hold the most recent output or goes to a pre-defined output.

Single Network I/O Pack Output Response to Loss of Input

Outputs	Frame 1	Frame 2	Frame 3
Health	Healthy		Unhealthy
Alarm			Send
Values	Hold last		Standby

3.6.4.2 Dual Network I/O Pack Output

When an output pack features two network inputs it responds to the loss of one network by using the output command from the other network. This selection takes place within the frame time and generates no observable fall-over time from the I/O pack. The command from the lost network is held for one frame and declared unhealthy in the second frame. An alarm is sent in the third frame.

Loss of First Input, Dual Network I/O Pack Output Response

Input Buffer	Frame 1	Frame 2	Frame 3
Health	Healthy		Unhealthy
Alarm			Send
Values	Hold last		Zero
Outputs			
Health	Healthy		
Values	2nd input		

When the second network is lost (both networks lost), the behavior is similar to the single network input pack. The output is held for the first frame after loss of command. In the second frame, the output moves to the defined condition and the output health is marked as bad. An alarm is generated in the third frame.

Loss of Second Input, Dual Network I/O Pack Output Response

Input Buffer	Frame 1	Frame 2	Frame 3
Health	Healthy		Unhealthy
Alarm			Send
Values	Hold last		Zero
Outputs			
Health	Healthy		Unhealthy
Values	Hold last		Standby

3.7 Failure Analysis Probability

Reliability parameters for a given SIF are calculated using Markov models and the appropriate failure rates from the Mark VIeS failure modes, effects, and diagnostic analysis (FMEDA). For low-demand mode applications the PFD_{avg} is calculated, while for high demand mode applications the PFH is calculated. In addition, the mean time to fail spurious (MTTFS) is calculated for both modes.

For the default Markov model calculation, the analysis assumes a SIF with three analog input, two digital input, and two digital output signals. The following table displays the results of the Markov model calculation for several Mark VIeS control configurations in low-demand mode applications. A proof test interval (PTI) of one, two, and three years is used, assuming a perfect proof test.

Markov Model Calculation for Several Mark VIeS Control Configurations

Configuration	PFD_{avg}			MTTFS [yrs]		
	PTI 1 yr	PTI 2 yr	PTI 3 yr	PTI 1 yr	PTI 2 yr	PTI 3yr
Simplex 1 out of 1	0.00412	0.0082	0.0123	20.3	20.39	20.47
Dual 1 out of 2	0.000126	0.000272	0.000438	10.27	10.29	10.31
Dual 2 out of 2	0.00348	0.0069	0.0103	15.79	15.77	15.75
TMR 2 out of 3	0.000147	0.000354	0.000616	300.63	193.09	145.12

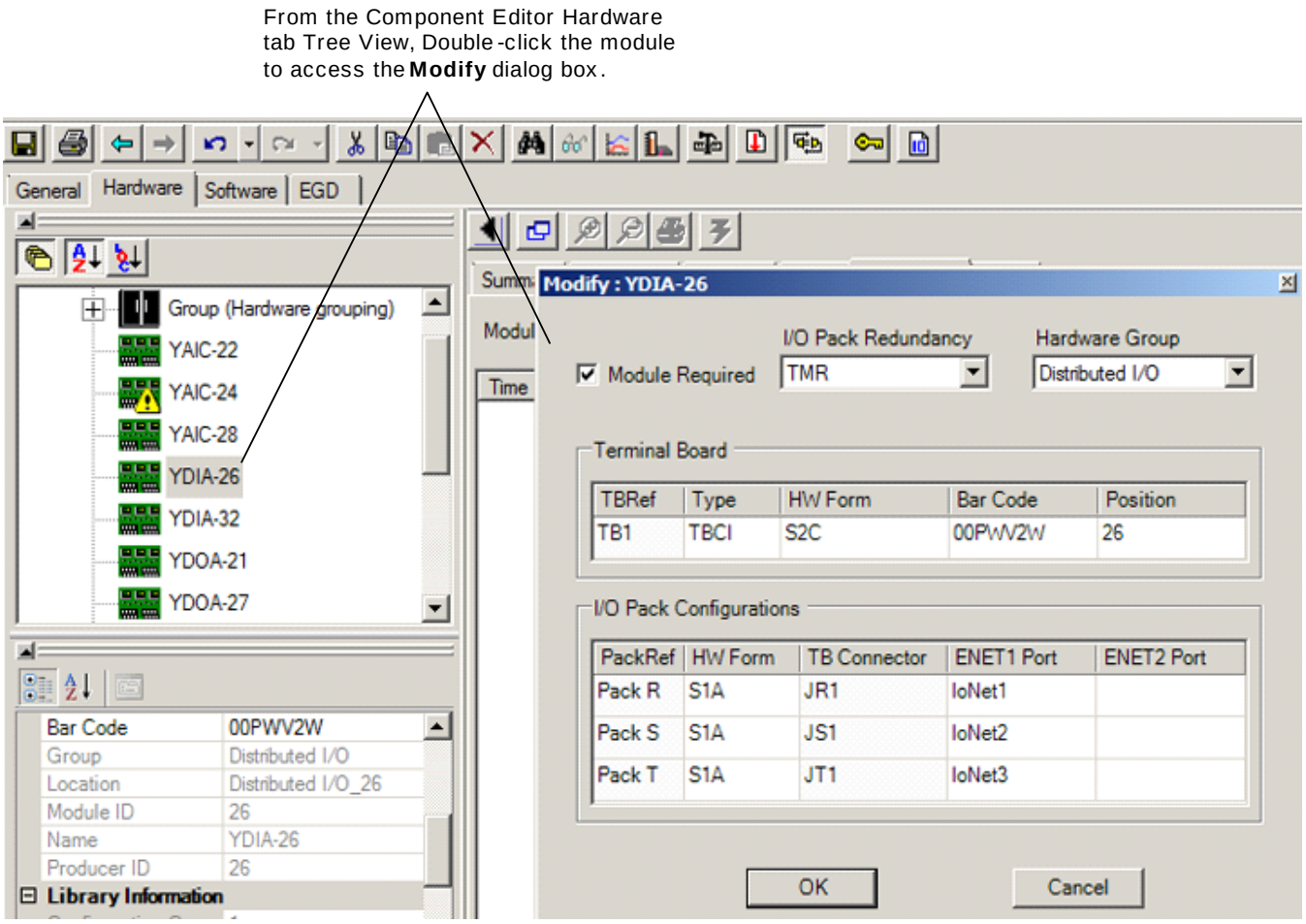
The following table displays the results of the Markov model calculation for two Mark VIeS Safety control configurations in high-demand mode applications.

Markov Model Calculation for Two Mark VIeS Control Configurations

Configuration	PFH [hr^{-1}]	MTTFS [yrs]
Dual 1 out of 2	0.0000000644	4.74
TMR 2 out of 3	0.0000000367	139.02

3.8 System Configuration

Prior to use, each I/O pack must be configured in the ToolboxST application.



Note When configuring I/O packs, be sure that the I/O pack configuration matches the hardware configuration of the attached terminal board. Refer to the chapter, *I/O Configuration* for detailed hardware and software configuration tables and checklists for Mark VIeS I/O packs and terminal boards. Use the checklists to cross-check the board configuration with the hardware topology.

3.8.1 YAIC Analog Input/Output

The Analog Input/Output (YAICS1A) pack provides the electrical interface between one or two IONets and a terminal board. The pack handles up to 10 analog inputs, the first 8 of which can be configured as ±5 V or ±10 V inputs, or 4-20 mA current inputs. The last two inputs can be configured as ±1 mA or 4-20 mA inputs. Using 4-20 mA inputs yields better DC than voltage inputs.

YAIC is compatible with the TBAIS1C and STAI terminal boards. YAIC is only compatible with the S1C version of TBAI and will report a board compatibility problem with any other version.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

3.8.1.1 TBAI Analog Input/Output

The Analog Input/Output (TBAI) terminal board holds 10 analog inputs and 2 outputs connected directly to two terminal blocks mounted on the board. Each block has 24 terminals that accept up to #12 AWG wires. A shield terminal attachment point is located adjacent to each terminal block.

The TBAI can hold the following inputs and outputs:

- Analog input -two-wire, three-wire, and four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ±5 V, ±10 V dc
- Analog output, 0-20 mA

A 24 V dc power supply is available on the terminal board for all transducers. The inputs can be configured as either voltage or current signals. The two analog output circuits are 4-20 mA. TBAI can be used with one or three YAIC I/O packs. Dual YAICs on TBAI are not supported.

TBAI I/O Capacity

Quantity	**Analog Input Types**
8	±10 V dc, or ±5 V dc, or 4-20 mA
2	4-20 mA, or ±1 mA
Quantity	**Analog Output Types**
2	0-20 mA

3.8.1.2 STAI Simplex Analog Input

The Simplex Analog Input (STAI) terminal board holds 10 analog inputs and 2 analog outputs connected to a high-density Euro-block type terminal block. STAI is designed for DIN-rail or flat mounting. It can hold the same inputs and outputs as the TBAI terminal board.

A 24 V dc power supply is available on the terminal board for all transducers. The inputs can be configured as either voltage or current signals. The two analog output circuits are 0-20 mA.

STAI Input Capacity

Quantity	**Analog Input Types**
8	±10 V dc, or ±5 V dc, or 4-20 mA
2	4-20 mA, or ±1 mA
Quantity	**Analog Output Types**
2	0-20 mA

3.8.2 YDIA Discrete Input

The Discrete Input (YDIAS1A) pack provides the electrical interface between one or two IONets and a terminal board. The I/O pack accepts up to 24 contact inputs and terminal board specific feedback signals, and supports three different voltage levels. YDIA is compatible with seven terminal boards.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

3.8.2.1 TBCI Contact Input with Group Isolation

The Contact Input with Group Isolation (TBCI) terminal board accepts 24 dry contact inputs wired to two barrier type terminal blocks. Dc power is provided for contact excitation. TBCI accepts one, two, or three YDIA packs. Three versions of TBCI are available.

TBCI Input Capacity

Terminal Board	Contact Inputs	Excitation Voltage
TBCIS1C	24	Nominal 125 V dc, floating, ranging from 100 to 145 V dc
TBCIS2C	24	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
TBCIS3C	24	Nominal 48 V dc, floating, ranging from 32 to 64 V dc

3.8.2.2 STCI Simplex Contact Input

The Simplex Contact Input (STCI) terminal board accepts 24 contact inputs wired to a Euro-block type terminal block. The STCI is designed for DIN-rail or flat mounting and accepts a single YDIA. Four versions of STCI are available.

STCI Input Capacity

Terminal Board	Contact Inputs	TB Type	Excitation Voltage
STCIS1A	24	Fixed	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
STCIS2A	24	Pluggable	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
STCIS4A	24	Pluggable	Nominal 48 V dc, floating, ranging from 32 to 64 V dc
STCIS6A	24	Pluggable	Nominal 125 V dc, floating, ranging from 100 to 145 V dc

3.8.3 YDOA Discrete Output

The Discrete Output (YDOAS1A) pack provides the electrical interface between one or two IONets and a terminal board. YDOA is capable of controlling up to 12 electromagnetic or solid-state relays and accepts terminal board specific feedback. YDOA is compatible with six terminal boards.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

3.8.3.1 TRLYS1B Relay Output with Coil Sensing

The Relay Output with coil sensing (TRLYS1B) terminal board accepts 12 relay outputs wired directly to two barrier type terminal blocks. Each block has 24 terminals that accept up to #12 AWG wires.

The first six relay circuits are jumper configurable either for dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115/230 V ac source, or an optional 24 V dc source, can be provided for field solenoid power. The next five relays are unpowered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications requiring dedicated power from connector JG1. TRLYS1B supports a single YDOA on connector JA1, or three YDOAs on connectors JR1, JS1, and JT1. The fuses should be removed for isolated contact applications to ensure that suppression leakage is removed from the power bus.

Note Jumpers JP1-JP6 are removed in the factory and shipped in a plastic bag. Re-install the appropriate jumper if power to a field solenoid is required. Conduct individual loop energized checks as per standard practices, and install the jumpers as required.

3.8.3.2 TRLYS1D Relay Output with Servo Sensing

The Relay Output with servo sensing (TRLYS1D) terminal board holds six plug-in magnetic relays wired to a barrier type terminal block. The six relay circuits are Form-C contact outputs, powered and fused to drive external solenoids. A standard 24 V dc or 125 V dc source can be used. TRLYS1D supports a single YDOA on connector JA1, or three YDOAs on connectors JR1, JS1, and JT1.

3.8.3.3 TRLYS#F Relay Output with TMR Contact Voting

The Relay Output with TMR contact voting (TRLYS1F) terminal board provides 12 contact-voted relay outputs. TRLYS1F holds 12 sealed relays in each TMR section, for a total of 36 relays among three boards. The relay contacts from R, S, and T are combined to form a voted Form A normally open (NO) contact. 24/125 V dc or 115 V ac power can be applied. Three YDOA packs plug into the JR1, JS1, and JT1 37-pin D-type connectors on the terminal board. TRLYS#F does not have power distribution or support simplex systems.

Note TRLYS2F is the same as TRLYS1F except that voted contacts form a Form B normally closed (NC) output.

3.8.3.4 SRLY Simplex Relay Output

The Simplex Relay Output (SRLY) terminal board provides 12 form C relay contact outputs wired to a Euro-style box terminal block. Each of 12 sealed relays uses an isolated contact set for relay position feedback. The SRLY accepts a single YDOA, which can have one or two network connections.

3.8.3.5 SRSA Simplex Compact Digital Output

The Simplex Compact Digital Output (SRSA) terminal board provides 10 relay outputs, grouped as bank A and bank B. Each bank contains 5 outputs as a series combination of force-guided relay contacts and a solid-state relay. The primary disconnect operation should use the solid-state relays. The mechanical relays, one for each bank, are provided for redundancy and safety purposes.

3.8.4 YHRA HART Enabled Analog Input/Output

The Highway Addressable Remote Transducer (HART) Enabled Analog Input/Output (YHRAS1A) pack provides the electrical interface between one or two IONets and a terminal board. The YHRA holds up to 10 analog inputs, the first 8 of which can be configured as ±5 V or 4-20 mA inputs. The last two inputs can be configured as ±1 mA or 4-20 mA current inputs. It also supports two 4-20 mA outputs.

While in 4-20 mA mode, the YHRA can relay HART messages between HART enabled field devices and an Asset Management System (AMS). These HART enabled devices can be connected through any of the inputs or outputs.

Attention

HART signals are for monitoring purposes only, and must be configured as non-interfering.

YHRAS1A is compatible with the SHRA terminal board and is capable of single I/O pack operation only. Refer to *Appendix A* for detailed hardware and software configuration tables and checklists for Mark VIeS I/O packs and terminal boards. Use the checklists to cross-check the board configuration with the hardware topology.

Attention

For proper operation, the YHRA ToolboxST parameter AMS_Msg_Only must be set to disable.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

3.8.4.1 SHRA Simplex HART Enabled Analog Input/Output

The Simplex HART Enabled Analog Input/Output (SHRA) terminal board accepts 10 analog inputs and two analog outputs wired to a high-density Euro-block type terminal board. Connected to the YHRA pack, SHRA allows HART messages to pass between the YHRA and a HART enabled field device. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 4-20 mA. SHRA accepts a single YHRA I/O pack.

3.8.5 YTCC Thermocouple Input

The Thermocouple Input (YTCCS1A) pack provides the electrical interface between one or two IONets and a terminal board. YTCC handles up to 12 thermocouple inputs, while two packs can handle 24 inputs on TBTCS1C. Type E, J, K, S, and T thermocouples can be used, and they can be grounded or ungrounded. YTCC is compatible with the TBTC or the STTC terminal boards. In TMR configuration with the TBTCS1B terminal board, three packs are used with three cold junctions, but only 12 thermocouples are available.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

Compatibility

Terminal Board	**TBTC**			**STTC**
Version and Inputs	TBTCS1B (12 TC) TBTCS1C (24 TC)*	TBTCS1B (12 TC)	TBTCS1B (12 TC)	STTCS1A (12 TC) STTCS2A
Pack Quantity	Single – Yes	Dual – Yes	Triple – Yes	Single – Yes
*Support of 24 thermocouple inputs on TBTC requires the use of two YTCC packs.				

3.8.5.1 TBTC Thermocouple Input

The Thermocouple Input (TBTC) terminal board accepts up to 24 type E, J, K, S, or T thermocouple inputs wired to two barrier type terminal blocks and connects to the YTCC pack. TBTC works with the YTCC pack in simplex, dual, and TMR systems. In simplex systems two YTCC packs plug into the TBTCS1C for a total of 24 inputs. With TBTSH1B, one, two, or three YTCC packs plug-in to support a variety of system configurations, but only 12 inputs are available.

3.8.5.2 STCC Simplex Thermocouple Input

The Simplex Thermocouple Input (STTC) terminal board accepts 12 thermocouples wired to a Euro-block type terminal block, and connects to the YTCC pack. The on-board signal conditioning and cold junction reference is identical to those on the larger TBTC board. STCC is designed for DIN-rail or flat mounting and accepts a single YTCC I/O pack.

3.8.6 YVIB Vibration Input

3.8.6.1 YVIBS1A

The Vibration Input (YVIBS1A) pack provides the electrical interface between one or two IONets and a terminal board. The pack handles up to 12 vibration inputs, the first 8 of which can be configured to read vibration or proximity inputs, channels 9-12 support proximeters only and channel 13 can input either a Keyphasor transducer or proximity-type signal. The terminal board also support non-safety rated buffered outputs of the input signal. The YVIBS1A I/O pack is rated SIL 1 with HFT of zero.

YVIBS1A is compatible with the TVBAS1A or TVBAS2A terminal board.

SIL Capability:

- SIL 1 in HFT = 0 architectures (1 out of 1, 2 out of 2)
- SIL 2 in HFT = 1 architectures (1 out of 2, 2 out of 3)

3.8.6.2 YVIBS1B

The Vibration Input (YVIBS1B) pack provides the electrical interface between one or two IONets and a terminal board. the pack handles up to 13 inputs. The first 8 can be configured to read vibration or proximity sensors, channels 9-11 support position sensors only, and channels 12 and 13 can be configured to support either position sensors or KeyPhasor transducers. The terminal board also supports non-safety buffered outputs of the input signals. The YVIBS1B I/O pack is rated SIL 2 with HFT of zero.

YVIBS1B is compatible with the TVBAS1A or TVBAS2A terminal boards.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 our of 1, 2 out of 2)
- SIL 3 in HFT = 1 architectures (1 our of 2, 2 out of 3)

3.8.6.3 TVBA Vibration Input

The Vibration Input (TVBA) terminal board provides 8 vibration inputs, 3 position inputs, an additional 2 position or Keyphasor inputs, and non-safety rated buffered outputs connected directly to two terminal blocks mounted on the board. Each block has 24 terminals that accept up to #12 AWG wires. A shield terminal attachment point is located adjacent to each terminal block. The TVBA can hold the following inputs and outputs:

- Vibration input Proximeters, Seismics, and Velomitor***** sensor channels 1-8; Accelerometers (channels 1, 2, and 3 only)
- Position inputs Proximeters channels 9-12 for YVIBS1A and channels 9-11 for YVIBS1B
- Keyphasor transducer input Proximiter sensor channel 13 for YVIBS1A and channels 12 & 13 for YVIBS1B
- Non-safety rated, buffered outputs of the inputs

The first eight inputs are jumper configured:

- Jumpers J1A through J8A
  - Seismic (S)
  - Prox or Accel (P, A)
  - Velomitor sensor (V)
- Jumpers J1B through J8B
  - Prox, Velomitor sensor or Accel (P, V, A)
  - Seismic (S)
- Jumpers J1C through J8C
  - PCOM provides N28 return path for power
  - OPEN no N28 return path through terminal board

3.8.6.4 WNPS Power Supply Daughterboard

Three redundant external power supplies provide the power for the TVBA. If one of the power supplies fails, the off line power supply can be replaced without bringing down the terminal board. To maintain this feature, the TVBA has three removable daughter cards to provide –28 to 28 V dc power converters. The daughter cards can be removed while the TVBA is online by disconnecting the I/O pack power (one at a time R, S or T), and removing the WNPS. The daughterboards are required to be mounted to meet all vibration and seismic standards.

3.8.7 YPRO Backup Turbine Protection

The Emergency Turbine Protection (YPROS1A) pack and associated terminal boards provide an independent backup overspeed protection system. They also provide an independent watchdog function for the primary control. A typical protection system consists of three TMR YPRO I/O packs mounted on separate SPRO terminal boards. A cable, with DC-37 connectors on each end, connects each SPRO to an emergency trip board, TREG. An alternate arrangement places three YPRO I/O packs directly on TREA for a single-board TMR protection system.

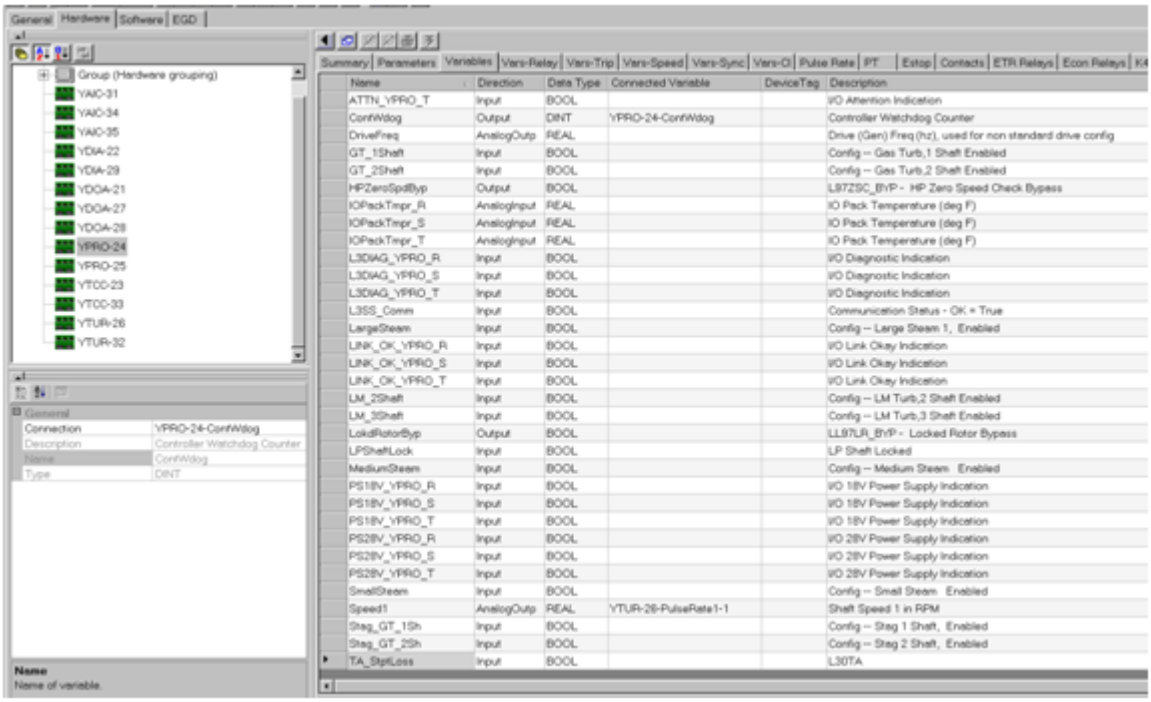
Mark VIeS control is designed with a primary and backup trip system that interacts at the trip terminal board level. Primary protection is provided with the YTUR pack operating a primary trip board (TRPG, TRPA). Backup protection is provided with the YPRO I/O pack operating a backup trip board (TREG, TREA).

YPRO accepts three speed signals, including basic overspeed, acceleration, deceleration, and hardware implemented overspeed. It monitors the operation of the primary control and can monitor the primary speed as a sign of normal operation. YPRO checks the status and operation of the selected trip board through a comprehensive set of feedback signals. The pack is fully independent of, and unaffected by, the controller operation. YPRO modules are complex in their configuration and operation and should only be installed and configured by qualified personnel familiar with turbine protection systems.

SIL Capability:

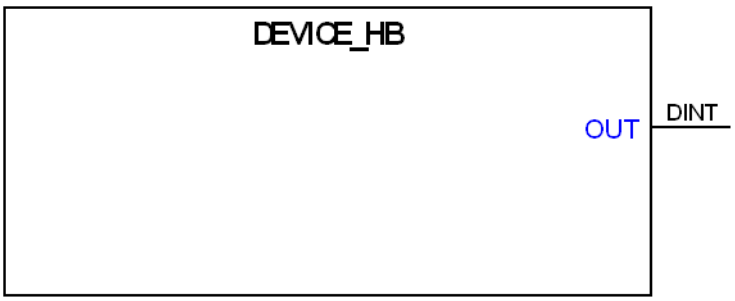
- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

In the ToolboxST application, when the YPRO variable *Speed1* is configured for either *StaleSpdEn* or *SpeedDifEn* (enabled), it must be connected to the controller's speed signal. An example is displayed in the following figure.



Connecting ContWdog and Speed1

For an additional LOP, YPRO expects a continuously updated output (*ContWdog*) from the controller. The variable *ContWdog Output* must be connected and programmed to be incremented each frame. If the value is not updated within five frames, YPRO generates a trip. This feature allows YPRO to independently verify that the application code continues to run in the controller.



Device_HB Block for ContWdog Counter

The YPRO I/O pack provides an additional LOP by monitoring the operating health of the system controller. The following rules apply if this protection is used:

- **Simplex main controller with TMR backup protection** is supported by all Mark VIeS backup trip boards (TREG and TREA). In this configuration, one port on each of three YPRO I/O packs connects to the controller IONet.
- **Dual Main Controllers with TMR backup protection** is supported by all Mark VIeS backup trip boards (TREG and TREA). This configuration uses the dual controller TMR output standard network connection. The first YPRO pack has one network port connected to the R IONet. The second pack has one network port connected to the S IONet. The third pack has one network port connected to the R IONet and one network port connected to the S IONet. The third YPRO monitors the operation of both controllers.
- **Triple Main Controllers with TMR backup protection** is supported when operating with a TMR main control (2 out of 3). All Mark VIeS backup trip boards (TREG and TREA) support this configuration. The network configuration connects the first YPRO pack to the R IONet, the second to the S IONet, and the third to the T IONet.

Note YPRO TMR applications do not support dual network connections for all three YPROs. In a redundant system there is no additional system reliability gained by adding network connections to the first two YPROs with dual controllers or any of the three YPROs with TMR controllers. The additional connections simply reduce mean time between failures (MTBF) without increasing mean time between forced outages (MTBFO).

3.8.7.1 TREA Turbine Emergency Trip

The Aeroderivative Turbine Emergency Trip (TREA) terminal board works with YPRO turbine I/O packs. The inputs and outputs are as follows:

- Nine passive pulse rate devices (three per X/Y/Z section) sensing a toothed wheel to measure the turbine speed
- Jumper blocks that enable one set of three speed inputs to be fanned to all three YPRO I/O packs
- Two 24 V dc (S1A, S3A) or 125 V dc (S2A, S4A) TMR voted output contacts to trip the system
- Four 24 to 125 V dc voltage detection circuits for monitoring trip string

For TMR systems, signals fan out to the JX1, JY1, and JZ1 DC-62 YPRO connectors.

3.8.7.2 TREG Turbine Emergency Trip

The Gas Turbine Emergency Trip (TREG) terminal board provides power to three emergency trip solenoids and is controlled by the YPRO. Up to three trip solenoids can be connected between the TREG and TRPG terminal boards. TREG provides the positive side of the 125 V dc to the solenoids and TRPG provides the negative side. YPRO provides emergency overspeed protection, emergency stop functions, and controls the 12 relays on TREG, nine of which form three groups of three to vote the inputs controlling the three trip solenoids.

3.8.7.3 SPRO Emergency Protection

The Emergency Protection (SPRO) terminal board hosts a single YPRO pack. It conditions speed signal inputs for the YPRO and contains a pair of potential transformers (PTs) for bus and generator voltage input. The DC-37 pin connector adjacent to the YPRO pack connector links the SPRO with a Mark VIeS trip board.

3.8.8 YSIL Core Safety Protection

The Core Safety Protection (YSIL) I/O pack and associated terminal boards provide an independent backup overspeed protection system. They also provide an independent watchdog function for the primary control (Mark VIeS controller). A protection system consists of three TMR YSIL I/O packs mounted onto a TSCA terminal boards. Three serial cables connect from the TSCA to three SCSAs.

Mark VIeS control is designed with a primary and backup trip system that interacts at the trip terminal board level. Primary protection is provided with the YTUR pack operating a primary trip board (TRPG, TRPA). Backup protection is provided with the YSIL I/O pack operating emergency trip relays (ETRs) on the TRPA.

YSIL accepts 12 speed signals (probes), including basic overspeed, acceleration, deceleration, and hardware implemented overspeed. It monitors the operation of the primary control (Mark VIeS controller) and can monitor the primary speed as a sign of normal operation. YSIL checks the status and operation of TSCA through a comprehensive set of feedback signals. The I/O pack is fully independent of, and unaffected by, the Mark VIeS controller operation.

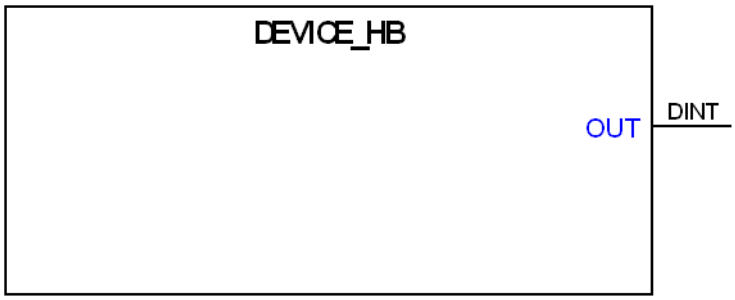
Note YSIL modules are complex in their configuration and operation and should only be installed and configured by qualified personnel familiar with turbine protection systems.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

In the ToolboxST application, when the YSIL variable *Speed1* is configured for either *StaleSpdEn* or *SpeedDifEn* (enabled), it must be connected to the controller's speed signal.

For an additional level of protection (LOP), YSIL expects a continuously updated output (*ContWdog*) from the controller. The variable *ContWdog Output* must be connected and programmed to be incremented each frame. If the value is not updated within five frames, YSIL generates a trip. This feature allows YSIL to independently verify that the application code continues to run in the controller.



Device_HB Block for ContWdog Counter

The YSIL I/O pack provides an additional LOP by monitoring the operating health of the system controller. The following rules apply if this protection is used:

- **Simplex main controller with TMR backup protection** is supported by the Mark VIeS backup trip board, TSCA. In this configuration, one port on each of three YSIL I/O packs connects to the controller IONet.
- **Dual Main Controllers with TMR backup protection** is supported by the Mark VIeS backup trip board, TSCA. This configuration uses the dual controller TMR output standard network connection. The first YSIL pack has one network port connected to the R IONet. The second pack has one network port connected to the S IONet. The third pack has one

network port connected to the R IONet and one network port connected to the S IONet. The third YSIL monitors the operation of both controllers.

- **Triple Main Controllers with TMR backup protection** is supported when operating with a TMR main control (2 out of 3). The Mark VIeS backup trip board, TSCA supports this configuration. The network configuration connects the first YPRO pack to the R IONet, the second to the S IONet, and the third to the T IONet.

Note YSIL TMR applications do not support dual network connections for all three YSILs. In a redundant system there is no additional system reliability gained by adding network connections to the first two YSILs with dual controllers or any of the three YSILs with TMR controllers. The additional connections simply reduce mean time between failures (MTBF) without increasing mean time between forced outages (MTBFO).

3.8.8.1 TCSA Turbine Emergency Trip

The TCSA uses the J2 connector to supply 125 V dc or 24 V dc power for ETRs 1-3 found on TB5 SOL1 & SOL2 and TB6 SOL3. Likewise, the J3 connector supplies power to ETRs 4-9 found on TB6 SOL4 - SOL9.

Under normal running conditions, the mechanical force-guided relay, K6 is energized and the ETRs 1,2 and/or 3 solid-state relays: ETR1-3 are energized. Similarly, the second mechanical force-guided relay, K7 is grouped with ETRs 4-6 and the third mechanical force-guided relay, K8 is grouped with ETRs 7-9. De-energizing any or all ETR(s) is considered a trip request.

3.8.8.2 SCSA I/O Expansion Board

The YSIL module requires three SCSA I/O expansion boards be connected through serial links to the TCSA terminal board. Each SCSA provides ten 4-20 mA inputs and ten 24 V dc transmitter power outputs, six 4-20 mA inputs for externally powered transmitters, three thermocouple inputs, three contact inputs, and three contact outputs. The YSIL can use any of the 4-20 mA analog inputs on the SCSA (AnalogInput01_R,S or T through AnalogInput16_R,S or T TMR input sets) in the Emergency Trip Relay (ETR) logic string.

3.8.9 YTUR Primary Turbine Protection

The Primary Turbine Protection (YTURS1A) pack provides the electrical interface between one or two IONets and a primary protection terminal board. YTUR plugs into the TTUR terminal board and handles four speed sensor inputs, bus and generator voltage inputs, shaft voltage and current signals, eight flame sensors, and outputs to the main breaker. Safety certified protection includes:

Speed An interface is provided for up to four passive, magnetic speed inputs with a frequency range of 2 to 20,000 Hz.

Flame Detection Voltage pulses above 2.5 V generate a logic high; the pulse rate is measured in a counter over a configurable time (multiple of 40 ms).

ETD TRPx contains relays for interface with the electrical trip devices (ETD).

Note For the Mark VIeS control, the flame sensing circuitry analysis was performed with the presence of flame considered as the safe state. YTUR flame sensing is not intended for applications where detected flame is the unsafe condition.

Attention

Only speed, flame detectors, ETD, and E-Stop circuits are certified for safety applications. All other functionality is non-safety rated.

YTURS1A is compatible with the TTUR and TRPA terminal boards. As an alternative to TTUR, three YTUR packs can be plugged directly into a TRPA terminal board. In this arrangement, TRPA holds four speed inputs per YTUR, or alternately fans the first four inputs to all three YTURs. TRPA provides two solid-state primary trip relays. This arrangement does not support bus and generator voltage inputs, shaft voltage or current signals, flame sensors, or main breaker output.

Note YTUR modules are complex in their configuration and operation, and should only be installed and configured by qualified personnel familiar with turbine protection systems.

SIL Capability:

- SIL 2 in HFT = 0 architectures (1 out of 1, 2 out of 2).
- SIL 3 in HFT = 1 architectures (1 out of 2, 2 out of 3).

3.8.9.1 TTUR Primary Turbine Protection Input

The Primary Turbine Protection Input (TTUR) terminal board works with the YTUR turbine I/O packs as part of the Mark VIeS control. Two barrier style terminal blocks accept the following inputs and outputs:

- Safety rated inputs and outputs:
  - Twelve pulse rate devices that sense a toothed wheel to measure turbine speed
  - Three overspeed trip signals to the trip board
- Non-safety rated inputs and outputs:
  - Generator voltage and bus voltage signals taken from PTs
  - 125 V dc output to the main breaker coil for automatic generator synchronizing
  - Shaft voltage and current inputs to measure induced shaft voltage and current

In simplex systems, YTUR mounts on connector JR4 and cable connects to TRPG through connector PR3. For TMR systems, signals fan out to the PR3, PS3, and PT3. TTUR supports connection of TRPG and TRPA boards through the JR4, JS4, and JT4 connectors.

Note TTUR configuration information refers to non-safety-related functions.

3.8.9.2 TRPG Turbine Primary Trip

The Gas Turbine Primary Trip (TRPG) terminal board is controlled by the YTUR. On two barrier style terminal blocks, TRPG holds nine magnetic relays in three voting circuits to interface with three trip solenoids (ETDs). The TRPG works with TREG to form the primary and emergency interface to the ETDs. TRPG holds inputs from eight Geiger-Mueller® flame detectors for gas turbine applications. There are two board types:

- The S1A and S1B version for TMR applications with three voting relays per solenoid
- The S2A and S2B version for simplex applications with one relay per solenoid

In Mark VIeS systems, the TRPG is controlled by YTUR packs mounted on a TTUR terminal board. The I/O packs plug into the D-type connectors on TTUR, which is connected by cable to TRPG.

Note In a dual-control mode topology where (1 out of 2) or (2 out of 2) tripping is desired, use YTUR with an externally wired TRPGS2 terminal board for the desired configuration.

3.8.9.3 TRPA Turbine Primary Trip

The Aeroderivative Turbine Primary Trip (TRPA) terminal board works with the YTUR turbine I/O packs or with the TTUR terminal board as part of the Mark VIeS system. Both TRPAS1A and TRPAS2A are compatible with YTUR. TRPA holds the following inputs and outputs on two barrier style terminal blocks:

- Twelve passive pulse rate devices (four per R/S/T section) that sense a toothed wheel to measure the turbine speed. Or, six active pulse rate inputs (two per TMR section)
- One 24 to 125 V dc fail-safe E-Stop input to remove power from trip relays
- Two 24 V dc (S1) or 125 V dc (S2) TMR voted output contacts to the main breaker coil for trip coil
- Four 24 to 125 V dc voltage detection circuits for monitoring trip string

For TMR systems, signals fan out to the PR3, PS3, PT3, JR4, JS4, and JT4 connectors. TRPA can be configured to provide 12 independent pulse rate speed inputs with 4 per YTUR or fan a single set of 4 inputs to all 3 YTUR packs. Jumpers JP1 and JP2 select the fanning of the four R section passive speed pickups to the S and T section YTURs. Unused jumpers are stored on passive headers located on the corner of the board.

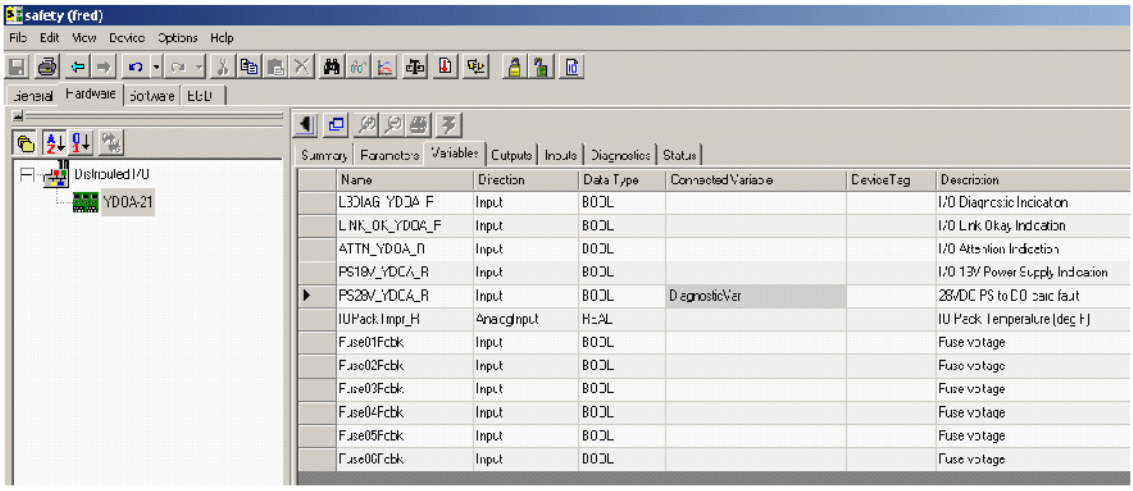
3.9 Power Sources

The Mark VIeS Safety control is designed to operate on a flexible selection of power sources. Power distribution modules (PDM) support the use of 115/230 V ac, 24 V dc, and 125 V dc power sources in many redundant combinations. The applied power is converted to 28 V dc for I/O pack operation. The controllers may operate from the 28 V dc I/O pack power or from direct 24 V dc battery power. Alternate power sources are acceptable if I/O pack power is regulated to be within ±5% of 28 V dc and overvoltage protection is provided by the power source. The extensive power feedback signals designed into the Mark VIe power distribution system are not critical to system safety but do provide useful information to assist in system maintenance.

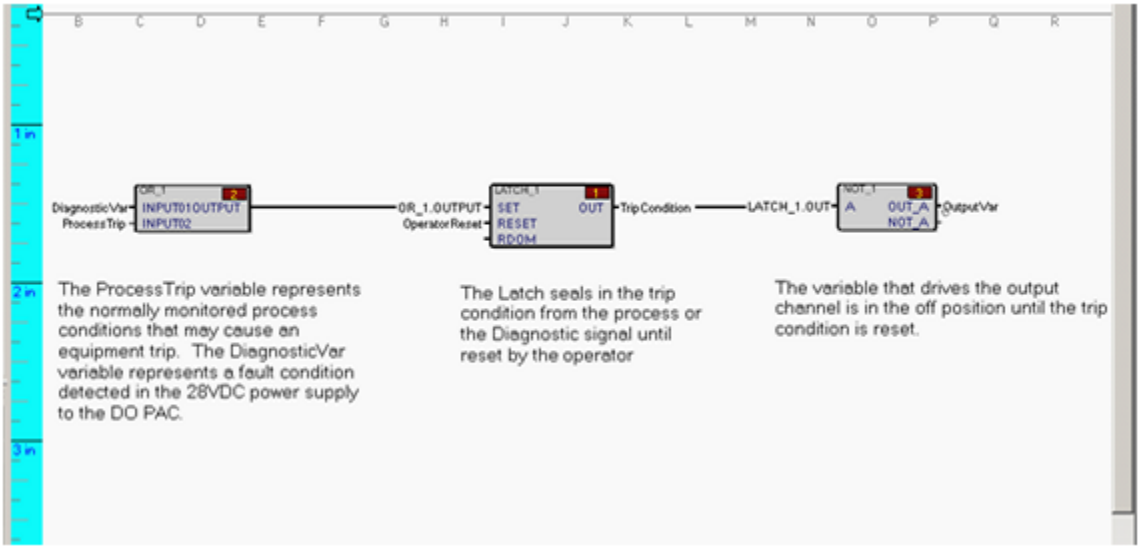
All Mark VIeS I/O packs include a circuit breaker at the 28 V dc power input that limits the available fault current. The breaker also provides soft-start, permitting the application of power to an I/O pack without concern for other connected loads. All I/O packs monitor input voltage for undervoltage conditions. The voltage monitoring function provides alarms at 25.1 V dc (28 V -5%) and 16 V dc.

When the input voltage drops below 25.1 V dc, an alarm is generated. The I/O pack continues to operate, but performance is degraded. For example, on terminal boards with 24 V dc power sources for powered field devices, the voltage begins to drop below 24 V dc and the available drive voltage for analog output is diminished. Action should be taken to begin an orderly shut-down of equipment protected by the affected SIFs. I/O pack operation will continue to permit a controlled shutdown.

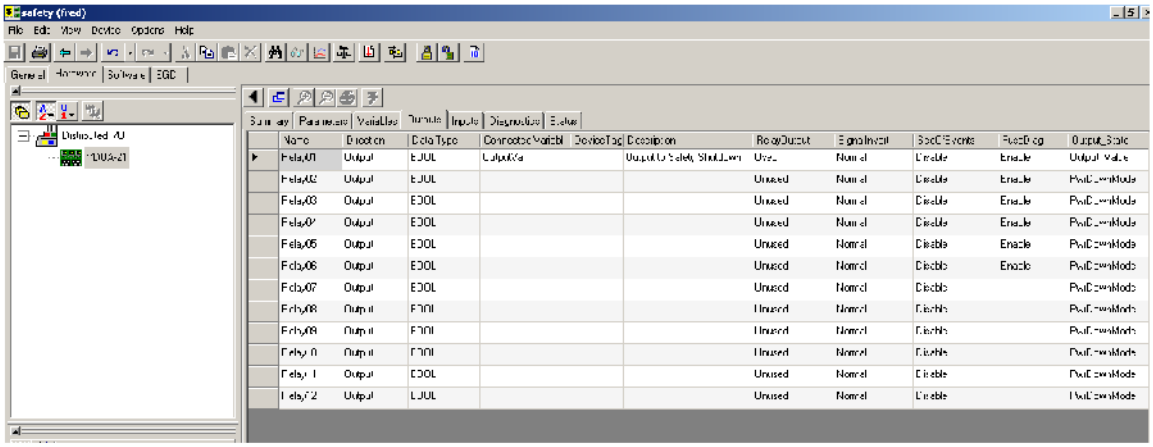
When the input voltage drops below 16 V dc, another alarm is generated. An output I/O pack enters its power-down state, the safe state for all but energize-to-trip SIFs. The following figures display an example of the power loss application in the ToolboxST application:



Input Variables



Controller Software Blocks



Output Variables

When designing de-energize-to-trip systems, the power circuits are not critical to safety because all failures are considered safe. This allows power systems with a single power distribution bus and supply to be used if it meets system running reliability requirements. For energize-to-trip systems, an interruption of all control power influences the ability to trip. To maintain an HFT of 1, three fully independent power supplies must be maintained for the redundant control electronics. The power distribution components available as part of the Mark VIe family provide the means to design a system with three separate control power distribution networks.

3.9.1 PPDA Power Distribution System Feedback

The PPDA I/O pack accepts inputs from up to six different power distribution boards. It conditions the board feedback signals and provides a dual-redundant Ethernet interface to the controllers. PPDA feedback is structured to be plug and play, using electronic IDs to determine the power distribution boards wired into it. This information then populates the IONet output to provide correct feedback from connected boards. For use with the Mark VIeS Safety controller, the PPDA I/O pack can be hosted by the JPDS, JPDC, or JPDM 28 V dc control power boards. It is compatible with the feedback signals created by JPDB, JPDE, and JPDF.

Caution

The PPDA I/O pack is not SIL-rated, and is authorized for use on a non-interfering basis for power system monitoring purposes only. PPDA feedback information cannot be used in a SIL-rated safety function.

Notes

4 Installation, Commissioning, and Operation

4.1 Installation

During installation, complete the following items:

- Documentation of a functional safety management plan, including:
  - Organization and resources
  - Risk evaluation and management to identify safety hazards
  - Safety planning, implementing, and monitoring
  - Functional safety assessment, auditing, and revisions
  - System configuration management
- Clear documentation of the required hardware and programmable logic for each safety loop
- Safety function validation tests plans
- Functional testing of each safety loop conducted under site environmental conditions
- Records of functional tests

4.2 Commissioning

During commissioning, the following items should be checked:

- All wiring is in accordance with design
- All software and firmware is up-to-date
- Test instrumentation is calibrated
- No diagnostics are present in hardware or software
- System is properly configured (configuration checklist verified)
- Power supplies are of proper type and in good working order
- All forcing points are removed prior to engaging Locked mode

4.3 Operation

To maintain safety integrity during normal operations, the following checks and periodic proof tests must be conducted to expose any DU hazards.

- Proof test intervals must be calculated for each SIF
- Proof tests must be conducted to ensure that the functional safety as designed is maintained and test results recorded
- All diagnostic alarms must be identified and corrected. Check the front lights on the I/O pack when performing this task.
- Contact GE if a fault is encountered.

4.3.1 Variable Health

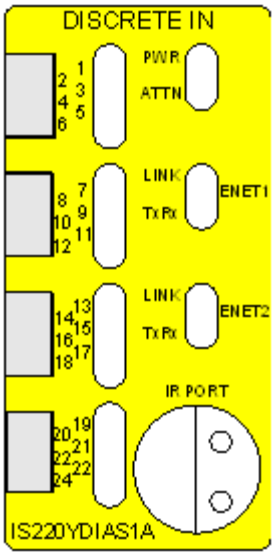
The Mark VIeS control detects I/O pack failures, defaults input data, and generates alarms as appropriate. The application code can be alerted to this type of failure by monitoring the health of critical input variables using the VAR_HEALTH block.

4.3.2 Alarming on Diagnostics

Alert an operator when a diagnostic alarm is active in the control system. Every pack and controller has a configuration variable *L3Diag* that is driven to the active state when there is an active diagnostic alarm in the device. Configure these variables as alarms in the application code so that they are available through the Alarm Viewer.

4.3.3 I/O Pack Status LEDs

During system operation, alarms or diagnostics must be promptly addressed. The following is a partial listing of I/O pack status LEDs.



A green LED labeled PWR indicates the presence of control power.
A red LED labeled ATTN indicates five different pack conditions as follows:

- LED out -no detectable problems with the pack
- LED solid on – a critical fault is present that prevents the pack from operating. Critical faults include detected hardware failures on the processor or acquisition boards, or no application code loaded.
- LED flashing quickly (¼ second cycle) – an alarm condition is present in the pack such as putting the wrong pack on the terminal board, or there is no terminal board, or there were errors loading the application code.
- LED flashing at medium speed (¾ second cycle) – the pack is not online
- LED flashing slowly (two second cycle) – the pack has received a request to flash the LED to draw attention to the pack. This is used during factory test or as an aid to confirm physical location against ToolboxST settings.

A green LED labeled LINK is provided for each Ethernet port to indicate that a valid Ethernet connection is present.

4.3.4 Restrictions

Restrictions in the Mark VIeS Safety control are as follows:

- The UCCCS05, UCSBS1A, and UCSCS2A are the only controller types certified for use in the Mark VIeS Safety control system.
  - UCCCS05 is in maintenance mode only in Mark VIeS V05.03 beginning with ControlST V07.02
  - UCSBS1A is supported beginning with ControlST V04.03 and higher
  - UCSCS2A is supported beginning with ControlST V07.02 and higher
  - UCCCS05
    - Does not support Modbus, and only supports 40, 80 and 160 ms frame periods
    - Compatible with all YxxxS1A and YxxxS1B I/O modules
  - UCSBS1A and UCSCS2A
    - Support both Modbus and the 10, 40, 80 and 160 ms frame periods
    - Compatible with all YxxxS1A I/O modules running at 40, 80 and 160 ms frame periods
    - Compatible with all YxxxS1B I/O modules running at 10, 40, 80 and 160 ms frame periods
  - Frame idle time must be above 30%. Frame idle time should be periodic as the set of operations implemented in a frame is fixed for a given configuration. It can be monitored for a controller using the FrameIdleTime_x intrinsic variables on Trender or calculating a minimum using blockware. Frame idle time is calculated in the controller every frame.

    Note To measure minimum frame idle time, measurements must be taken with all inputs healthy and separately with at least one input module unhealthy (for example, with the Ethernet cable removed from the I/O module). In most cases, the scenario with at least one input module unhealthy will have a lower frame idle time.

  - Average system idle time must be above 30%. System idle time is not periodic because of many features that are interrupt-based rather than frame based, such as UDH EGD consumption, communications with ToolboxST/HMI, and so forth. System idle time can be monitored for a controller using the IdleTime_x intrinsic variables on Trender and is calculated as a 1 second average. It is acceptable for measured system idle time to dip below 30%, but this must only occur less than 10% of the time.
  - At frame periods of 40, 80 and 160 ms, any combination of the Safety I/O modules is allowed, up to a maximum of 50 modules per IONet
  - At a frame period of 10 ms, any combination of Safety I/O modules is allowed such that all frame input clients complete within 1.6 ms after the start of the frame

    ---

    Note 1.6 ms allows for a required 20% safety margin.

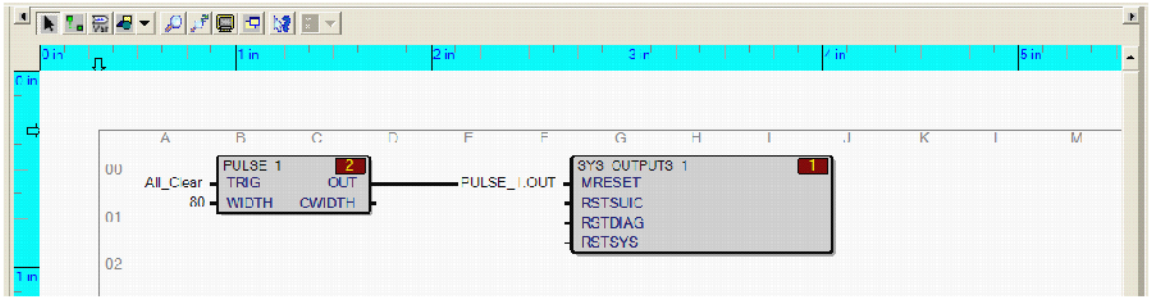
    Execution time of the frame input clients varies based on the following user configurable items:

    - Controller type
    - Number of I/O modules
    - Types of I/O modules
    - Number of voted Boolean variables
    - Number of voted Analog variables

    For additional information, refer to the Appendix, *Determine Frame Input Client Completion Time*.

- Use only GE approved Ethernet switches in the Mark VIeS Safety control I/O network.
- The YHRA can be used for analog I/O requiring the HART communications interface. HART communications should be used for monitoring only and not for control.

- The analog outputs of the YHRA are NOT capable of hardware TMR voting and can only be applied as a simplex output. HART communications can be configured for simplex mode input only (no HART multi-drop support).
- The YHRA configuration parameter *AMS_Msg_Only* must be set to disable.
- YVIBS1A is SIL 1 rated with an HFT of 0, SIL 2 with an HFT of 1.
- YVIB buffered outputs are not safety-certified.
- SRLY optional fused power distribution card WROx may only be used for power distribution, fuse diagnostic feedback signals are not safety certified.
- TRLY-F optional fused power distribution card WPDF may only be used for power distribution, fuse diagnostic feedback signals are not safety certified.
- IR interface to the I/O packs is prohibited while functioning as a safety control.
- The Mark VIeS Safety control allows communication with other controllers and Human-machine Interface (HMI) devices through the UDH protocol. The UDH communication channel is not safety-certified so any data accessed from UDH and used within a safety loop should be verified by the application code using appropriate measures. Commands from the HMI devices (for example setpoint changes) are not accepted by the Mark VIeS control.
- The presence of active diagnostic alarms in the control system indicates that safety functions may be compromised. All diagnostics should be cleared prior to startup and any diagnostic that occurs should be attended to in a timely fashion.
- Feedback values from the PPDA cannot be used for SIL-rated safety functionality. The PPDA is approved for non-interfering, power distribution system monitoring purposes only.
- The YTUR flame detection has been designed and analyzed with the safe state being the presence of flame. Flame sensing is not intended for applications where detected flame is the unsafe state.
- The master reset should be cleared before engaging safety control. The Master Reset command is issued by the controller to the I/O packs to reset any existing trips or suicide latches. If the fault condition remains after the reset has been issued, the trip or suicide is issued again. Because the I/O packs evaluate the Master Reset command at each run cycle, the I/O packs toggle between the cleared and faulted condition if the command remains active for an extended time and a persistent fault condition is present. To prevent this, the Master Reset command must be pulsed to the I/O packs and remain active for at least two frames before returning to the inactive state. The following figure displays the application code that implements this function.



Pulsed Master Reset

4.4 Product Life

During operation and maintenance, the following product life guidelines should be followed:

- The I/O packs have no known wear-out mechanism and do not require periodic maintenance.
- There are no wear items on the UCSBS1A or UCSCS2A controllers similar to the I/O packs.
- The terminal boards have no known wear-out mechanism and do not require periodic maintenance.
- The bulk 28 V dc power supplies have internal capacitors with finite life. Replacement of the power supplies should be scheduled every 15 years.
- The recommended Ethernet switches have internal power supply capacitors with finite life. Replacement of the switches should be scheduled every 15 years.
- Capacitor life predictions are based on an average ambient temperature of 35ºC (95 ºF). Capacitor life is reduced by ½ for every 10ºC (18 ºF) of average temperature above 35ºC (95 ºF).
- The cooling fan in the UCCC CPCI controller rack has a specified service life of 80,000 hours at 40ºC (104 ºF). Replacement should be scheduled within this time period.
- The lithium battery for the UCCC has a service life of 10 years. The battery is disabled in stock and can be disabled when storing a controller. If it is desired to keep the local time-of-day clock operational through power interruptions, the Mark VIeS Safety controller battery should be replaced following the schedule below. This time-of-day is not critical to the safety function, and is overwritten by system time service in many applications. If the controller is stored with the battery disabled, its life expectancy is 10 years, minus the time the controller has been in service. If the controller is stored with the battery enabled, the life expectancy drops to seven years minus the time the controller has been in service.
- The power supply in the UCCC CPCI rack has internal capacitors with finite life. Replacement of the power supply should be scheduled every 15 years.
- The UCCC CPCI rack backplane has capacitor filtering with finite life. Replacement of the backplane should be scheduled every 15 years.

Notes

5 I/O Configuration

This chapter contains tables that should be used as checklists for I/O point configuration. Copies of each table should be made and the appropriate values either checked or written in the final column. The ToolboxST module configuration should be verified against the installed I/O module hardware.

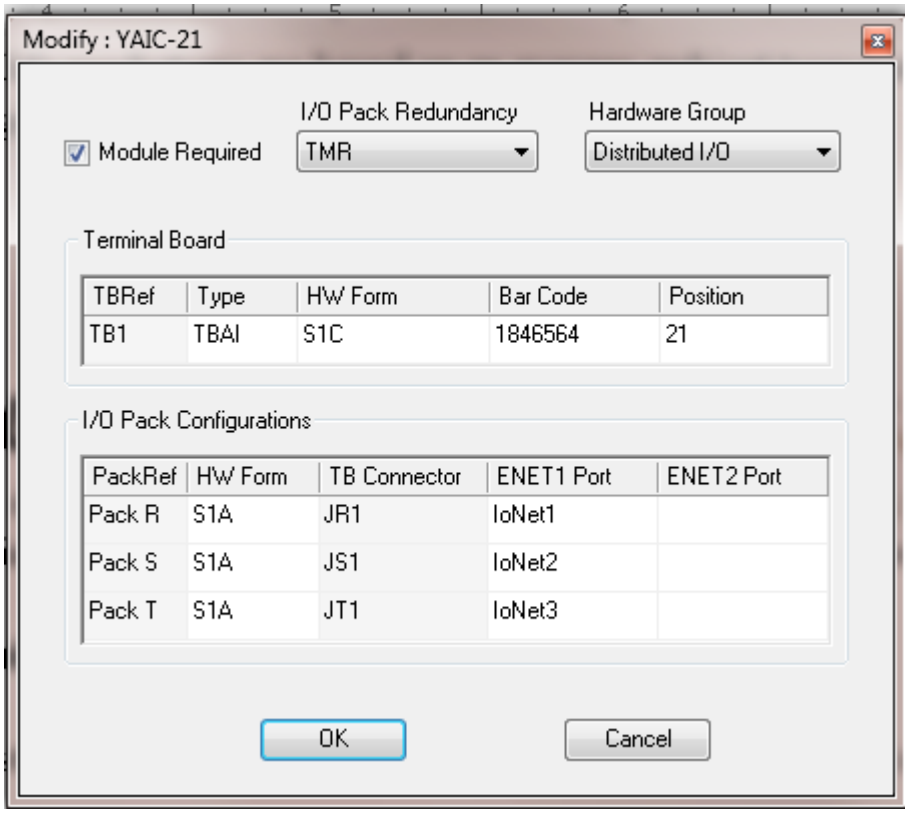
➢ To verify terminal board configuration

1. Upon initial installation, prior to securing the module cover, locate and record the terminal board information.

a. The terminal board part number contains the Type and Form information.

IS200 TBAI S1C
[Type] [Form]

b. Record the terminal board barcode. This must be entered into the ToolboxST module configuration if offline or there is an ellipse that can automatically detect this ID if online.



5.1 YAIC

5.1.1 YAIC Compatibility

The YAIC I/O pack contains an internal processor board.

- The YAICS1A contains a BPPB processor board. This processor has a limited component lifecycle, with support up to firmware V04.06.

Attention

From the ToolboxST application, do not upgrade YAICS1A to firmware above V04.06. YAICS1A is not supported in firmware V05.00 or later.

- The YAICS1B contains a BPPC processor board that is supported by firmware V05.01 or later with ControlST***** Software Suite V06.01 or later.

Attention

YAICS1A and YAICS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All three YAIC I/O packs in a TMR set must be the same hardware form.

YAIC I/O pack is compatible with the TBAISIC and STAIS#A terminal boards.

Terminal Board	I/O Pack Redundancy		
	Simplex	Dual	TMR
TBAIS1C	Yes	No	Yes
STAIS#A	Yes	No	No

- Simplex uses one I/O pack with one or two IONet connections.
- TMR uses three I/O packs with a separate IONet connection on each pack.

5.1.2 YAICS1B Configuration

5.1.2.1 Parameters

Parameter	Description	Choices
SystemLimits	Enable or *temporarily* disable all system limit checks. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 22.5 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 22.5 mA

5.1.2.2 Inputs

Input	Description	Choices
AnalogInput01 through AnalogInput10	First of 10 Analog Inputs – board point. Point edit	(Input REAL)
InputType	Current or voltage input type	Unused or 4-20 mA (for all Analog Inputs) ±5 V or ±10 V (for AnalogInput01 to 08 only) ±1 mA (for AnalogInput09 and 10 only)
Low_Input	Value of input current (mA) or voltage (V) at low end of input scale	-10 to 20
Low_Value	Value of input in engineering units at Low_Input	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of input current (mA) or voltage (V) at high end of input scale	-10 to 20
High_Value	Value of input in engineering units at High_Input	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused, 0.75hz, 1.5hz, 3hz, 6hz, 12hz
TMR_DiffLimit	Difference limit for voted inputs in % of High_Value - Low_Value	0 to 200
SysLim1Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim1Latch	System Limit 1 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim1Type	System Limit 1 Check Type	>= or <=
SysLim1	System Limit 1 in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Enable System Limit 1 fault check	Enable, Disable
SysLim2Latch	System Limit 2 fault latch - if set, requires a Reset System Limits (RSTSYS) on SYS_OUTPUTS block to clear	Latch, NotLatch
SysLim2Type	System Limit 2 Check Type	>= or <=
SysLimit2	System Limit 2 in Engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enables the generation of a high limit diagnostic alarm when the value of the 4-20 mA input is greater than the value of parameter *Max_MA_Input*	Enable, Disable
DiagLowEnab	Enables the generation of a low limit diagnostic alarm when the value of the 4-20 mA input is less than the value of parameter *Min_MA_Input*	Enable, Disable
TMR_DiffLimt	Diag limit, TMR input vote difference, in percent of (High_Value - Low_Value)	0 to 200 %

5.1.2.3 Outputs

Output Name	Output Description	Choices
AnalogOutput01 - AnalogOutput02	First of two analog outputs - board point, Point edit	Output REAL
Output_MA	Output current, mA selection.	Unused, 0-20 mA
OutputState	State of the outputs when offline. When the PAIC loses communication with the controller, this parameter determines how it drives the outputs: PwrDownMode - Open the output relay and drive outputs to zero current HoldLastVal - Hold the last value received from the controller Output_Value - Go to the configured output value set by the parameter Output_Value	PwrDownMode HoldLastVal Output_Value
Output_Value	Pre-determined value for the outputs	-3.4082 e + 038 to 3.4028 e + 038
Low_MA	Output mA at low value	0 to 200 mA
Low_Value	Output in Engineering Units at Low_MA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 200 mA
High_Value	Output value in Engineering Units at High_MA	-3.4082 e + 038 to 3.4028 e + 038
TMR_Suicide	Enables suicide for faulty output current, TMR only	Enable, Disable
TMR_SuicLimit	Suicide threshold (Load sharing margin) for TMR operation, in mA	0 to 200 mA
D/A_ErrLimit	Difference between D/A reference and feedback, in % for suicide, TMR only	0 to 200 %
Dither_Ampl	Dither % current of Scaled Output mA	0 to 10
Dither_Freq	Dither rate in Hertz	Unused, 12.5hz, 25hz, 33.33hz, 50hz, 100hz

5.1.2.4 Variables

Variable Name	Description	Direction	Type
L3DIAG_YAIC	Board diagnostic	Input	BOOL
LINK_OK_YAIC	I/O Link OK indication	Input	BOOL
ATTN_YAIC	Module Diagnostic	Input	BOOL
IOPackTmpr	I/O Pack Temperature (deg F)	Input	REAL
PS18V_YAIC	I/O 18V Power Supply Indication	Input	BOOL
PS28V_YAIC	I/O 28V Power Supply Indication	Input	BOOL
SysLimit1_1	System Limit 1	Input	BOOL
↓	↓	Input	BOOL
SysLimit1_10	System Limit 1	Input	BOOL
SysLimit2_1	System Limit 2	Input	BOOL
↓	↓	Input	BOOL
SysLimit2_10	System Limit 2	Input	BOOL
OutSuicide1	Status of Suicide Relay for Output 1	Input	BOOL
OutSuicide2	Status of Suicide Relay for Output 2	Input	BOOL
Out1MA	Feedback, Total Output Current, mA	Input	REAL
Out2MA	Feedback, Total Output Current, mA	Input	REAL

5.1.3 YAICS1A Configuration

The ToolboxST application configured items should be verified against the selected terminal board configuration.

YAIC Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex TMR
Hardware group		Distributed I/O Group
Terminal board	Terminal board type/form/barcode	
I/O pack configurations	Pack form/TB Connector/IONet	

Parameters Tab

Configuration	Description	Select Option ✓ or Enter Value
SystemLimits	Enable or disable system limits	Enable Disable
Min_MA_Input	Select minimum current for healthy 4-20 mA input	0 to 21 mA
Max_MA_Input	Select maximum current for healthy 4-20 mA input	0 to 21 mA

Input Tab (repeat for 10 inputs)

Input	Description	Select Option ✓ or Enter Value
InputType	Current or voltage input type	Unused 4-20 mA ±5 V ±10 V ±1 mA (Inputs 9 and 10)
Low_Input	Value of current at the low end of scale	-10 to 20
Low_Value	Value of input in engineering units at low end of scale	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of current at the high end of scale	-10 to 20
High_Value	Value of input in engineering units at high end of scale	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused 0.75 Hz 1.5 Hz 3.0 Hz 6.0 Hz 12.0 Hz
SysLim1Enabl	Input fault check	Enable Disable
SysLim1Latch	Input fault latch	Latch Unlatch
SysLim1Type	Input fault type	≥ ≤
SysLim1	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Input fault check	Enable Disable
SysLim2Latch	Input fault latch	Latch Unlatch
SysLim2Type	Input fault type	≥ ≤
SysLim2	Input limit in engineering Units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enable high input limit diagnostic	Enable Disable
DiagLowEnab	Enable low input limit diagnostic	Enable Disable
TMRDiffLimt	Diagnostic limit, TMR input vote difference, in percent of (High_Value – Low_Value)	0 to 200 %

Analog Output Tab (repeat for 2 outputs)

Output	Description	Select Option ✓ or Enter Value
Output_MA	Type of output current, mA selection	Unused 0 – 20 mA
OutputState	State of the outputs when offline	PwrDownMode Hold Last Value Output_Value
Output_Value	Pre-determined value for the outputs	
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in engineering units at low mA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in engineering units at high mA	-3.4082 e + 038 to 3.4028 e + 038
TMRSuicide	Suicide for faulty output current, TMR only	Enable Disable
TMRSuicLimit	Suicide threshold for TMR operation	0 to 20 mA
D/AErrLimit	Difference between D/A reference and output, in % for suicide, TMR only	0 to 100 %
DitherAmpl	Dither % current of scaled output mA	0 to 10
Dither_Freq	Dither rate in hertz	Unused 12.5 Hz 25.0 Hz 33.33 Hz 50.0 Hz 100.0 Hz

TBAI Terminal Board

TBAI Circuit	Jumper	Select ✓
Input 1	J1A	V dc
		20 mA
	J1B	Open
		Ret
Input 2	J2A	V dc
		20 mA
	J2B	Open
		Ret
Input 3	J3A	V dc
		20 mA
	J3B	Open
		Ret
Input 4	J4A	V dc
		20 mA
	J4B	Open
		Ret
Input 5	J5A	V dc
		20 mA
	J5B	Open
		Ret
Input 6	J6A	V dc
		20 mA
	J6B	Open
		Ret
Input 7	J7A	V dc
		20 mA
	J7B	Open
		Ret
Input 8	J8A	V dc
		20 mA
	J8B	Open
		Ret
Input 9	J9A	V dc
		20 mA
	J9B	Open
		Ret

TBAI Terminal Board (continued)

TBAI Circuit	Jumper	Select ✓
Input 10	J10A	V dc
		20 mA
	J10B	Open
		Ret
Circuit	**Jumper**	
Output 1	Must be set to 20 mA only	
Output 2	No jumper – 20 mA only	

STAI Terminal Board

STAI Circuit	Jumper	Select ✓
Input 1	J1A	V dc
		20 mA
	J1B	Open
		Ret
Input 2	J2A	V dc
		20 mA
	J2B	Open
		Ret
Input 3	J3A	V dc
		20 mA
	J3B	Open
		Ret
Input 4	J4A	V dc
		20 mA
	J4B	Open
		Ret
Input 5	J5A	V dc
		20 mA
	J5B	Open
		Ret
Input 6	J6A	V dc
		20 mA
	J6B	Open
		Ret
Input 7	J7A	V dc
		20 mA
	J7B	Open
		Ret

STAI Terminal Board (continued)

STAI Circuit	Jumper	Select ✓
Input 8	J8A	V dc
		20 mA
	J8B	Open
		Ret
Input 9	J9A	V dc
		20 mA
	J9B	Open
		Ret
Input 10	J10A	V dc
		20 mA
	J10B	Open
		Ret
Output 1	Must be set to 20 mA only	
Output 2	No jumper – 20 mA only	

5.2 YDIA

5.2.1 YDIA Compatibility

The YDIA I/O pack contains an internal processor board.

- The YDIAS1A contains a BPPB processor board. This processor has a limited component lifecycle, with support up to firmware V04.06 only.

Attention

From the ToolboxST application, do not upgrade YDIAS1A to firmware above V04.06. YDIAS1A is not supported in firmware V05.00 and later.

- The YDIAS1B contains a BPPC processor board that is supported by firmware V05.01 or later with ControlST Software Suite version 6.01 or later.

Attention

YDIAS1A and YDIAS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All YDIA I/O packs in a TMR or DUAL set must be the same hardware form.

The YDIA I/O pack is compatible with seven discrete contact input terminal boards, including the TBCI boards and STCI boards.

I/O Pack Redundancy	Terminal Board
Simplex, Dual, or TMR	TBCIS1, S2, S3
Simplex only	STCIS1A, S2A, S4A, and S6A

Module redundancy refers to the number of I/O packs used in a signal path, as follows:

- Simplex uses one I/O pack with one or two network connections.
- Dual uses two I/O packs with one network connection on each.
- TMR uses three I/O packs with one network connection on each.

5.2.2 Parameters

Parameter	Description	Choices
ContactInput	Mark a specific contact input as Used or Unused.	Used, Unused
SignalInvert	Inversion makes signal true if contact is open	Normal, Invert
SeqOfEvents	Record contact transitions in sequence of events	Enable, Disable
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, Disable
Signal Filter	Contact input filter in milliseconds	Zero, Ten, Twenty, Fifty, Hundred

5.2.3 Inputs

Input	Direction	Type
Contact01	Input	BOOL
↓	↓	↓
Contact24	Input	BOOL

5.2.4 Variables

Note The following variable names are displayed differently depending on redundancy of I/O pack (R, S, or T) and if this is a PDIA or YDIA pack.

Variable	Description	Direction	Type
L3DIAG_PDIA_x L3DIAG_YDIA_x	I/O diagnostic indication, where x is R, S, or T	Input	BOOL
LINK_OK_PDIA_x LINK_OK_YDIA_x	I/O link okay indication, where x is R, S, or T		BOOL
ATTN_PDIA_x ATTN_YDIA_x	I/O attention indication, where x is R, S, or T		BOOL
IOPackTmpr_x	I/O pack temperature, where x is R, S, or T		REAL
PS18V_PDIA_x PS18V_YDIA_x	I/O 18 V power supply indication, where x is R, S, or T		BOOL
PS28V_PDIA_x PS28V_YDIA_x	I/O 28 V power supply indication, where x is R, S, or T		BOOL

5.2.5 YDIAS1A Configuration

YDIA Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex Dual TMR
Hardware group		Distributed I/OGroup
Terminal board	Terminal board type/form/barcode	
I/O pack configurations	Pack form/TB Connector/IONet	

Parameters Tab

Parameters	Description	Select Option ✓ or Enter Value
SystemLimits	Enable or disable system limit	Enable Disable

Application Digital Input Tab (repeat for 24 inputs)

Input	Description	Select Option ✓ or Enter Value
ContactInput		Used Not Used
SignalInvert	Inversion makes signal true if contact is open. Do not rely on the SignalInvert property of digital inputs to invert the value. Implement this operation in the application code with the input connected to a NOT block.	Normal Invert
SeqOfEvents	Record contact transitions in sequence of events	Enable Disable
DiagVoteEnab	Enable voting disagreement diagnostic	Enable Disable
SignalFilter	Contact input filter in milliseconds	Zero Ten Twenty Fifty Hundred

5.3 YDOA

5.3.1 YDOA Compatibility

The YDOA I/O pack contains an internal processor board.

- The YDOAS1A contains a BPPB processor board. This processor has a limited component lifecycle, with support up to firmware V04.11.

Attention

From the ToolboxST application, do not upgrade YDOAS1A to firmware above V04.11. YDOAS1A is not supported in firmware V05.00 or later.

- The YDOAS1B contains a BPPC processor board that is supported by firmware V05.00 or later with ControlST***** Software Suite V06.01 or later.

Attention

YDOAS1A and YDOAS1B I/O pack versions cannot be mixed on the same T-type terminal board.

All three YDOA I/O packs in a TMR set must be the same hardware form.

YDOA is compatible with several types of discrete (relay) output terminal boards.

Terminal Board	Description	Module Redundancy
TRLYS1B	Relay output with coil sensing	Simplex or TMR
TRLYS1D	Relay output with solenoid integrity sensing	
TRLYS1F, S2F	Relay output with TMR contact voting	TMR
SRLYS1A, S2A	Form C contact relays	Simplex
SRSAS1A, S3A	Compact size with normally open relays For hardware availability, contact the nearest GE Sales or Service Office, or an authorized GE Sales Representative. Compatible with YDOAS1B firmware V05.00 or later Compatible with the YDOAS1A firmware V04.11	Simplex

5.3.2 YDOA Configuration

YDOA Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex TMR
Hardware group		Distributed I/O Group
Terminal board	Terminal board type/form/barcode	
I/O pack configurations	Pack form/TB Connector/IONet	

5.3.3 Inputs

Parameter	Description	Select Option or Enter Value
ContactInput	Enables Relay#Fdbk	Unused, Used
SignalInvert	Inverts Relay#Fdbk signal and Relay#ContactFdbk signal (if available) **Do not rely on the SignalInvert property of digital inputs to invert the value. Implement this operation in the application code with the input connected to a NOT block.**	Normal, Invert
SeqOfEvents	Record RelayFdbk transitions in sequence of events Not available with TRLY#D.	Disable, Enable
DiagVoteEnab	Enable voting disagreement diagnostic	Disable, Enable
SignalFilter	Relay feedback digital filter in milliseconds, is only available with TRLYH#C (not available for safety use)	Zero, Ten, Twenty, Fifty, Hundred

5.3.4 Outputs

Parameter	Description	Select Option or Enter Value
RelayOutput	Enable relay output	Used, Unused
SignalInvert	Inversion makes relay closed if signal is false **Do not rely on the SignalInvert property of digital inputs to invert the value. Implement this operation in the application code with the input connected to a NOT block.**	Normal, Invert
SeqOfEvents	Record relay command transitions in sequence of events	Disable, Enable
FuseDiag	Enable fuse diagnostic (if available)	Enable, Disable
Output_State	Select the state of the relay condition based on I/O pack going offline with controller	PwrDownMode, HoldLastValue, Output_ Value
Output_Value	Pre-determined value for the outputs (only displayed if Output_State is set to Output_Value)	Off, On

5.3.5 Variables

Name	Description	Direction	Type
L3DIAG_PDOA_x L3DIAG_YDOA_x	I/O diagnostic indication, where x = R, S, or T	Input	BOOL
LINK_OK_PDOA_x LINK_OK_YDOA_x	I/O link okay indication, where x = R, S, or T	Input	BIT
ATTN_PDOA_x ATTN_YDOA_x	I/O Attention Indication, where x = R, S, or T	Input	BIT
IOPackTmpr_x	I/O pack temperature, where x = R, S, or T	Input	REAL
†Cap1_Ready_x	I/O pack capture buffer 1 ready for upload (currently not used), where x = R, S, or T	Input	BIT
†Cap2_Ready_x	I/O pack capture buffer 2 ready for upload (currently not used), where x = R, S, or T	Input	BIT
†CV_Permissive	CV (control valve) permissive for PGEN PLU function	Input	BIT
†IV_Permissive	IV (intercept valve) permissive for PGEN PLU function	Input	BIT
† Not applicable to YDOA			

Name	Description	Direction	Type
Relay#	Relay# output command	Output	BIT
Relay#Fdbk	Relay# Driver Status (set of 12 relays)	Input	BIT
Relay#ContactFdbk	Relay# Contact Status (set of 12 relays), available for TRLY#C, TRLY#E, SRSA, and SRLY only	Input	BIT
Fuse#Fdbk	Fuse voltage (if available)	Input	BIT
Solenoid#Status	Solenoid# Resistance Sense (set of 6 relays), True means resistance within the range, False means resistance out of the range, available for TRLY#D only	Input	BIT

TRLYS1B

Jumper	Select ✓
JP1	Excited DRY
JP2	Excited DRY
JP3	Excited DRY
JP4	Excited DRY
JP5	Excited DRY
JP6	Excited DRY

5.4 YHRA

YHRA Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex
Hardware group		Distributed I/O Group
Terminal board	Terminal board type/form/barcode	
I/O pack configurations	Pack form/TB Connector/IONet	

Parameters Tab

Parameter	Description	Select Option ✓ or Enter Value
SystemLimits	Enable or disable system limits	Enable Disable
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 21 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 21 mA
AMS_Msg_Priority	AMS messages have priority over controlled messages.	Enable Disabled
AMS_Msgs_Only	AMS messages only, do not send any control messages. Generates alarm 160 when enabled.	Enable Disabled
AMS_Mux_Scans_ Permited	Allow AMS scan commands for Hart message one and two. Hart message three is always allowed.	Enable Disable
Min_MA_HART_ Output	Minimum current sent to a HART enabled port. HART COMM will not be possible during offline modes if value is set < 4 mA	0 to 22.5

Analog Input Tab (repeat for 10 inputs)

YHRA Input	Description	Select Option ✓ or Enter Value
InputType	Current or voltage input type	Unused 4-20 mA ±5 V
Low_Input	Value of current at the low end of scale	-10 to 20
Low_Value	Value of input in engineering units at low end of scale	-3.4082 e + 038 to 3.4028 e + 038
High_Input	Value of current at the high end of scale	-10 to 20
High_Value	Value of input in engineering units at high end of scale	-3.4082 e + 038 to 3.4028 e + 038
InputFilter	Bandwidth of input signal filter	Unused 0.75 1.5 Hz 3 Hz 6 Hz 12 Hz
Hart_Enable	Allow the HART Protocol on this I/O point. This must be set to TRUE if HART messages are needed from this field device	Enable Disable
Hart_CtrlVars	Number of variables to read from the device. Set to zero if not used.	0 to 5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0 to 26
Hart_MfgID	HART field device's manufacturers code. A diagnostic alarm is sent if the field device ID differs from this value and the value is non-zero. This value can be uploaded from the YHRA if the field device is connected. (Right-click on device name and select Update HART IDS.)	0 to 255
Hart_DevType	HART field device – Type of device. (Refer to Hart_MfgID)	0 to 255
Hart_DevID	HART field device – Device ID. (Refer to Hart_MfgID)	0-116777215
SysLim1Enabl	Input fault check	Enable Disable
SysLim1Latch	Input fault latch	Latch Unlatch
SysLim1Type	Input fault type	≥ ≤
SysLim1	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
SysLim2Enabl	Input fault check	Enable Disable
SysLim2Latch	Input fault latch	Latch Unlatch
SysLim2Type	Input fault type	≥ ≤

Analog Input Tab (repeat for 10 inputs) (continued)

YHRA Input	Description	Select Option ✓ or Enter Value
SysLim2	Input limit in engineering units	-3.4082 e + 038 to 3.4028 e + 038
DiagHighEnab	Enable high input limit	Enable Disable
DiagLowEnab	Enable low input limit	Enable Disable

Analog Output Tab (repeat for 2 outputs)

YHRA Output	Description	Select Option ✓ or Enter Value
Output_MA	Type of output current, mA selection	Unused Enabled
Standby_State	State of the outputs when offline	PwrDownMode Hold Last Value Output_Value
Output_Value	Pre-determined value for the outputs	
Low_MA	Output mA at low value	0 to 20 mA
Low_Value	Output in engineering units at low mA	-3.4082 e + 038 to 3.4028 e + 038
High_MA	Output mA at high value	0 to 20 mA
High_Value	Output value in engineering units at high mA	-3.4082 e + 038 to 3.4028 e + 038
D/AErrLimit	Difference between D/A reference and output, in %	0 to 100 %
Hart_Enable	Allow the HART protocol on this I/O point. This must be set to TRUE if HART messages are needed from this field device	Enable Disable
Hart_CtrlVars	Number of variables to read from the device. Set to zero if not needed for control.	0 to 5
Hart_ExStatus	Number of extended status bytes to read from the device. Set to zero if not needed for control.	0 to 26
Hart_MfgID	HART field device's Manufacturers ID.	0 to 255
Hart_DevType	HART field device – Type of device. (Refer to Hart_MfgID)	0 to 255
Hart_DevID	HART field device – Device ID. (Refer to Hart_MfgID)	0-116777215

SHRA (JP1A – JP10A and JP1B – JP10B)

Circuit	Jumper	Select ✓
Input 1	J1A J1B	V dc 20 mA Open Ret
Input 2	J2A J2B	V dc 20 mA Open Ret
Input 3	J3A J3B	V dc 20 mA Open Ret
Input 4	J4A J4B	V dc 20 mA Open Ret
Input 5	J5A J5B	V dc 20 mA Open Ret
Input 6	J6A J6B	V dc 20 mA Open Ret
Input 7	J7A J7B	V dc 20 mA Open Ret
Input 8	J8A J8B	V dc 20 mA Open Ret
Input 9	J9A J9B	1 mA 20 mA Open Ret
Input 10	J10A J10B	1 mA 20 mA Open Ret

5.5 YTCC

5.5.1 YTCC Configuration

Parameter	Description	Choices
	Parameters	
SysFreq	System frequency (used for noise rejection)	50 or 60 Hz
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable, Disable
Auto Reset	Automatic restoring of thermocouples removed from scan	Enable, Disable
	Thermocouples	
ThermCplType	Select thermocouples type or mV input Unused inputs are removed from scanning, mV inputs are primarily for maintenance, but can also be used for custom remote CJ compensation. Standard remote CJ compensation also available.	Unused, mV, T,K,J, E, or S
ThermCplUnit	Select thermocouples display unit in °C or °F. This value needs to match units of attached variable. The ThermCplUnit parameter affects the native units of the controller application variable. It is only indirectly related to the tray icon and associated unit switching capability of the HMI. This parameter should not be used to switch the display units of the HMI.  ***Caution*** **Do not change the ThermCplUnit parameter because these changes will require corresponding changes to application code and to the Format Specifications or units of the connected variable. This parameter modifies the actual value sent to the controller as seen by application code. Application code that is written to expect degrees Fahrenheit will not work correctly if this setting is changed. External devices, such as HMIs and Historians, may also be affected by changes to this parameter**	deg_F, deg_C
LowPassFiltr	Enable 2 Hz low pass filter	Enable, Disable
SysLimit1	System Limit 1 in °C, °F, or mV	-60 to 3500 (FLOAT)
SysLim1Enabl	Enable system limit 1 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable
SysLim1Latch	Latch system limit 1 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch	NotLatch, Latch
SysLim1Type	System limit 1 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	≥ or ≤
SysLimit2	System Limit 2 in °C, °F, or mV	-60 to 3500 (FLOAT)

Parameter	Description	Choices
SysLim2Enabl	Enable system limit 2 fault check, a temperature limit which can be used to create an alarm.	Enable, Disable
SysLim2Latch	Latch system limit 2 fault Determines whether the limit condition will latch or unlatch; reset used to unlatch System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤) a preset value	NotLatch, Latch
SysLim2Type	System limit 2 check type limit occurs when the temperature is greater than or equal (≥), or less than or equal to (≤), a preset value	≥ or ≤
TMR_DiffLimt	Diagnostic limit, TMR input vote difference in engineering units Limit condition occurs if three temperatures in R, S, T differ by more than a preset value (engineering units); this creates a voting alarm condition.	-60 to 3500 (FLOAT)

5.5.1.1 YTCC Cold Junctions

Cold junctions are similar to thermocouples but without low pass filters.

Cold Junction Name	Cold Junction Description	Choices
ColdJuncType	Select CJ Type	Remote, Local
ColdJuncUnit	Select TC Display Unit Deg °C or °F. Value needs to match units of attached variable	Deg_F, Deg_C
SysLimit1	System Limit 1 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim1Enabl	Enable System Limit 1 Fault Check	Disable, Enable
SysLim1Latch	Latch System Limit 1 Fault	NotLatch, Latch
SysLim1Type	System Limit 1 Check Type (≥ or ≤)	≥ or ≤
SysLimit2	System Limit 2 - Deg °F or Deg °C	-40 to 185 (FLOAT)
SysLim2Enabl	Enable System Limit 2 Fault Check	Disable, Enable
SysLim2Latch	Latch System Limit 2 Fault	NotLatch, Latch
SysLim2Type	System Limit 2 Check Type (≥ or ≤)	≥ or ≤
TMR_DiffLimt	Diag Limit, TMR Input Vote Difference, in Eng Units	-60 to 3500 (FLOAT)

5.5.1.2 YTCC Variables

I/O Points (Signals)

Points (Signals)	Description - Point Edit (Enter Signal Connection Name)	Direction	Type
L3DIAG_YTCC	I/O diagnostic indication	Input	BIT
LINK_OK_YTCC	I/O link okay indication	Input	BIT
ATTN_YTCC	I/O attention indication	Input	BIT
IOPackTmpr	I/O pack temperature	Input	FLOAT
SysLim1TC1	System limit 1 for thermocouple 1	Input	BIT
:	:	Input	BIT
SysLim1TC12	System limit 1 for thermocouple 12	Input	BIT
SysLim1CJ1	System limit 1 for cold junction	Input	BIT
SysLim2JC1	System limit 2 for cold junction	Input	BIT
SysLim2TC1	System limit 2 for thermocouple 1	Input	BIT
:	:	Input	BIT
SysLim2TC12	System limit 2 for thermocouple 12	Input	BIT
CJBackup	Cold junction backup	Output	FLOAT
CJRemote1	Cold junction remote	Output	FLOAT
Thermocouple01	Thermocouple reading	Output	FLOAT
:	:	Output	FLOAT
Thermocouple12	Thermocouple reading	Output	FLOAT
ColdJunction1	Cold junction for TCs 1-12	Output	FLOAT

5.6 YVIB

5.6.1 YVIB Compatibility

There are currently two version of the I/O pack as follows:

- The YVIBS1A contains a BPPB processor board and two application boards. These internal boards have reached end of life.
- The YVIBS1B contains a BPPC processor board and a single application board. This I/O pack is supported with ControlST V06.01 or later. YVIBS1B supports an additional KeyPhasor input, a CDM input, and other Enhanced processing capabilities.

Attention

YVIBS1A and YVIBS1B cannot be mixed on a TMR module.

YVIBS1A is compatible with firmware versions up to V04.06.03C. Do NOT upgrade beyond this version.

If upgrading to YVIBS1B with an existing YVIBS1A configuration, use the ToolboxST application to correct the GAP12 configuration. Refer to the replacement procedure for detailed instructions.

For existing YVIBS1A applications after upgrading to YVIBS1B, the user may need to use the configurable low-pass filter to roll-off responses to match existing peak-to-peak calculations. This is because the YVIBS1B has an increased input signal bandwidth of 4500 Hz.

The following table provides a summary of compatibility for the YVIBS1A and YVIBS1B I/O pack versions.

Summary of Differences in YVIB Versions

Revision	Processor‡	Application Board(s)‡	YVIB Firmware Version	Supported ToolboxST Version	Required Mark VIe Controller Firmware Version	Enhanced Signal Mode	Channels / Sensor Types
YVIBS1A	BPPB	BAFA KAPA	V04.06.03C is the maximum supported firmware version. Do **Not** upgrade beyond this version.	Any	Any	No	13 / (S1A is different) *Supported Sensor Inputs*
YVIBS1B	BPPC	BBAA	Requires a full upgrade to ControlST Software Suite V06.02 or later			Yes	13 / (S1B is different) *Supported Sensor Inputs*
‡These boards are internal to the I/O pack and are not replaceable.							

The following table displays the available sensor types per channel with respect to the two different version of YVIB.

YVIB Supported Sensor Inputs

Sensor Type	Typical Application	YVIB Channel	
		YVIBS1A	YVIBS1B
Accelerometer	Aero-derivative gas turbines	1 - 8	1 - 8
Dynamic pressure probe	Land-Marine (LM) and Heavy-duty gas turbines (HDGT)	N/A	1 - 8
Proximitors* (Vibration)	Radial or axial measurements of turbine-driven generators, compressors, and pumps.	1 - 8	1 - 8
Velomitor*	Structural Vibration (mounted to case)	1 - 8	1 - 8
Pedestal or slot-type Keyphasor*	Rotor velocity and phase measurements	13	12, 13
Seismics	Structural Vibration (mounted to case)	1 - 8	1 - 8
Proximitors (Position)	Axial measurements	1-13	1-13

The YVIB I/O pack is compatible with the Vibration Terminal Board (TVBA) with simplex or TMR module redundancy.

YVIB and TVBA Compatibility

Terminal Board	Description	# of I/O Packs
TVBAS1A	Does not have buffered outputs IEC 61805 with YVIB I/O pack(s)	one or three
TVBAS2A	Provides buffered outputs and output connections IEC 61805 with YVIB I/O pack(s)	one or three

5.6.2 YVIBS1B Configuration

5.6.3 Component Editor

5.6.2.1 Parameters

Parameter	Description	Choices
SystemLimits	Allows user to temporarily disable all system limit checks for testing purposes. Setting this parameter to Disable will cause a diagnostic alarm to occur.	Enable (default) Disable
OperatingMode	Legacy is the backwards compatibility mode for PVIBH1A Enhanced enables enhanced algorithms for PVIBH1B and YVIBS1B that are not compatible with PVIBH1A, including Low Latency Peak-Peak Algorithm and Vibration RMS Algorithm	Legacy (default) Enhanced
Vib_PP_Fltr	First order filter time constant (sec) — cannot be disabled	0.01 to 2 (default is 0.10)
MaxVolt_Prox	Maximum Input Volts (pk-neg), healthy Input, Prox	-4 to 0 (default is -1.5)
MinVolt_Prox	Minimum Input Volts (pk-neg), healthy Input, Prox	-24 to -16 (default is -18.5)
MaxVolt_KP	Maximum Input Volts (pk-neg), healthy Input, Keyphasor	-4 to 0 (default is -1.5)

Parameter	Description	Choices
MinVolt_KP	Minimum Input Volts (pk-neg), healthy Input, Keyphasor	-24 to -16 (default is -22.0)
MaxVolt_Seis	Maximum Input Volts (pk-pos),healthy Input,Seismic:Values > 1.25 require use of GnBiasOvride	0 to 2.75 (default is 1.0)
MinVolt_Seis	Minimum Input Volts (pk-neg),healthy Input,Seismic:Values < -1.25 require use of GnBiasOvride	-2.75 to 0 (default is -1.0)
MaxVolt_Acc	Maximum Input Volts (pk),healthy Input,Accel	-12 to 1.5 (default is -8.5)
MinVolt_Acc	Minimum Input Volts (pk-neg),healthy Input,Accel	-24 to -1 (default is -11.5)
MaxVolt_Vel	Maximum Input Volts (pk),healthy Input,Velomitor	-12 to 1.5
MinVolt_Vel	Minimum Input Volts (pk-neg),healthy Input,Velomitor	-24 to -1
MaxVolt_CDM_BN	Maximum Input Volts (pk),healthy Input,CDM Bently Nevada	-12 to 24
MinVolt_CDM_BN	Minimum Input Volts (pk-neg),healthy Input,CDM Bently Nevada	-24 to 12
MaxVolt_CDM_PCB	Maximum Input Volts (pk),healthy Input,CDM PCB	-12 to 24
MinVolt_CDM_PCB	Minimum Input Volts (pk-neg),healthy Input,CDM PCB	-24 to 12
CDM_Scan_Period	The scan period for CDM sensor inputs in seconds Only assign as 0.01 increments	0.01 to 2.0

5.6.2.2 Variables

Variables	Description	Direction and Datatype
L3DIAG_xxxx_x	I/O Pack Diagnostic Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy of pack	Input BOOL
LINK_OK_xxxx_x	IONet Link Okay Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
ATTN_xxxx_x	I/O Pack Status Indicator where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
PS18V_xxxx_x	I/O Pack 18 V Power Supply Indication where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
PS28V_xxxx_x	I/O Pack 28 V Power Supply Indication where Pxxx or Yxxx is the name of the I/O pack and R, S, or T is the redundancy	Input BOOL
IOPackTmpr_	I/O Pack Temperature at the processor where R, S, or T is the redundancy	Input BOOL
RPM_KPH1	Speed (RPM)of KP#1,calculated from input#13	Analog Input REAL
RPM_KPH2	Speed (RPM)of KP#2,calculated from input#12 (PVIBH1B only)	Analog Input REAL
LM_RPM_A	Speed A(RPM), calculated externally to the I/O Pack	Analog Output REAL
LM_RPM_B	Speed B(RPM), calculated externally to the I/O Pack	Analog Output REAL
LM_RPM_C	Speed C(RPM), calculated externally to the I/O Pack	Analog Output REAL
SysLim1GAPx where x = 1 to 13	Boolean set TRUE if System Limit 1 exceeded for Gap x input	Input BOOL

Variables	Description	Direction and Datatype
SysLim2GAPx where x = 1 to 13	Boolean set TRUE if System Limit 2 exceeded for Gap x input	Input BOOL
SysLim1VIBx where x = 1 to 8	Boolean set TRUE if System Limit 1 exceeded for Vib x input	Input BOOL
SysLim2VIBx where x = 1 to 8	Boolean set TRUE if System Limit 2 exceeded for Vib x input	Input BOOL
SysLim1ACCx where x = 1 to 9	Boolean set TRUE if System Limit 1 exceeded for Accelerometer x input	Input BOOL
SysLim2ACCx where x = 1 to 9	Boolean set TRUE if System Limit 2 exceeded for Accelerometer x input	Input BOOL

5.6.2.3 Probe Nominal Settings

Probe Type	Gain †	Snsr_Offset (Vdc)	Scale (typical value)
Proximity	1x	9	200 mv/mil
Seismic	4x	0	150 mv/ips
Velomitor	2x	12	100 mv/ips
Accelerometer	2x	10	150 mv/ips
Keyphasor	1x	9	200 mv/mil
Bently Nevada CDM	2x	10	170 mv/psi
PCB CDM	2x	-12	170 mv/psi
†These are the default settings used if GnBiasOvride=Disable.			

5.6.2.4 LM 1–3

[ ] = defaults

Name	Direction	Data Type	Description	TMR_DiffLimit	SysLim1E-nabl	SysLim1-Latch	SysLimit1Type	SysLimit1
LMVib#A ↓ LMVib#C	AnalogInput	REAL	Magnitude of 1X harmonic relative to LM_RPM_A, B, or C calculated from input#1, 2, or 3 (9 total inputs)	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – Vibration in mils (prox) or Inch/sec (seismic,acel) [50] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – Vibration in mils (prox) or Inch/sec (seismic,acel) [0] -100 to 100

5.6.2.5 Vib1x 1-8

Name	Direction	Data Type	Description
VIB_1X1	AnalogInput	REAL	Magnitude of 1X harmonic relative to key phasor speed calculated from input#1
↓	↓	↓	↓
VIB_1X8	AnalogInput	REAL	Magnitude of 1X harmonic relative to key phasor speed calculated from input#8
Vib1xPH1	AnalogInput	REAL	Angle of 1X harmonic relative to key phasor calculated from input#1
↓	↓	↓	↓
Vib1xPH8	AnalogInput	REAL	Angle of 1X harmonic relative to key phasor calculated from input#8

5.6.2.6 Vib2x 1-8

Name	Direction	Data Type	Description
VIB_2X1	AnalogInput	REAL	Magnitude of 2X harmonic relative to key phasor speed calculated from input#1
↓	↓	↓	↓
VIB_2X8	AnalogInput	REAL	Magnitude of 2X harmonic relative to key phasor speed calculated from input#8
Vib2xPH1	AnalogInput	REAL	Angle of 2X harmonic relative to key phasor calculated from input#1
↓	↓	↓	↓
Vib2xPH8	AnalogInput	REAL	Angle of 2X harmonic relative to key phasor calculated from input#8

5.6.2.7 Vib 1-8

[ ] = defaults

Name	Direction	Data Type	Description	VIB_CalcSel	TMR_DiffLimt	Filter Type	Filtrhpcutoff
VIB1	AnalogInput	REAL	Vibration displacement (pk-pk) or velocity (pk), AC component of input#1	[VIB_Pk-Pk] Vib_RMS ‡	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Filter used for Velomitor and Seismic only [None], Low Pass, High Pass, Band Pass	High Pass 3db point (cutoff in Hz) [6] 4 to 300
↓	↓	↓	↓				
VIB8	AnalogInput	REAL	Vibration displacement (pk-pk) or velocity (pk), AC component of input#8				
‡Vib_RMS is only valid when OperatingMode is Enhanced and when using a PVIBH1B or YVIBS1B							

fltrlpattn	Filtrlpcutoff	fltrlppattn	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Slope or attenuation of high pass filter after cutoff [2-pole], 4-pole, 6-pole, 8-pole, 10-pole	Low Pass 3db point (cutoff in Hz) [500] 15 to 4300	Slope or attenuation of low pass filter after cutoff [2-pole] 4-pole, 6-pole, 8-pole, 10-pole	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=], <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [50] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=], <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [0] -100 to 100

5.6.2.8 Gap 1-3

[ ] = defaults
†is only valid with PVIBH1B or YVIBS1B
‡ LM Tracking Filter magnitude value may be inaccurate at 160, 320 ms frame periods.

Name	Direction	Data Type	Description	VIB_Type4	Scale	Scale_Off	TMR_ DiffLimit
GAP1_VIB1	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#1	Type of vibration probe, group 4 †CDM_BN_ChgAmp, †CDM_PCB_ ChgAmp, PosProx, [Unused], ‡VibLMAccel, VibProx, VibProx-KPH1, VibProx-KPH2, VibSeismic, VibVelomitor	Volts/-mil or Volt-s/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
GAP2_VIB2	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#2				
GAP3_VIB3	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#3				

GnBiasOvride	Snsr_Offset	Gain	LMIpcutoff	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Low pass 3dB point (cutoff Hz) for LM tracking filters 1.5Hz, 2.0Hz, [2.5Hz], 3.0Hz, 3.5Hz, 4.0Hz, 4.5Hz, 5.0Hz	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2	CDM_Probe_Gain	CDM_Amp_Gain
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100	PCB Probe Gain, pico-coulombs per psi [17] 1 to 100	PCB Charge amplifier Gain, millivolts per pico-coulomb [10] 1 to 100

5.6.2.9 Gap 4-8

[ ] = defaults
†is only valid with PVIBH1B or YVIBS1B

Name	Direction	Data Type	Description	VIB_Type	Scale	Scale_Off	TMR_ DiffLimit
GAP4_VIB4	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#4	Type of vibration probe, group 1 †CDM_BN_ChgAmp, †CDM_PCB_ ChgAmp, PosProx, [Unused], VibLMAccel, VibProx, VibProx-KPH1, VibProx-KPH2, VibSeismic, VibVelomitor	Volts/-mil or Volt-s/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
↓	↓	↓	↓				
GAP8_VIB8	AnalogIn-put	REAL	Average Air Gap (for Prox) or DC volts(for others),DC component of input#8				

GnBiasOvr-ide	Snsr_Offset	Gain	SysLim1E-nabl	SysLim1-Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2	CDM_Probe_Gain	CDM_Amp_Gain
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100	PCB Probe Gain, pico-coulombs per psi [17] 1 to 100	PCB Charge amplifier Gain, millivolts per pico-coulomb [10] 1 to 100

5.6.2.10 Gap 9-11

[ ] = defaults

Name	Direction	Data Type	Description	VIB_Type2	Scale	Scale_Off	TMR_ DiffLimit
GAP9_POS1	AnalogInput	REAL	Average Air Gap,DC component of input#9	Sensor Type, group 2 [Unused], PosProx	Volts/mil or Volts/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100
GAP10_POS2	AnalogInput	REAL	Average Air Gap,DC component of input#10				
GAP11_POS3	AnalogInput	REAL	Average Air Gap,DC component of input#11				

GnBiasOvride	Snsr_Offset	Gain	SysLim1Enabl	SysLim1Latch	SysLim1Type	SysLimit1
Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], 2x, 4x, 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100

5.6.2.11 KPH

[ ] = defaults
† is only valid with PVIBH1B or YVIBS1B

Name	Direction	Data Type	Description	VIB_Type3	Scale	Scale_Off	TMR_ DiffLimit	KPH_Thrshld
GAP12_KPH2	AnalogIn-put	REAL	Average Air Gap,DC component of input#9	Sensor Type, group 3 [Unused], PosProx, † KeyPhasor	Volts/-mil or Volt-s/ips [0.2] 0 to 2	Scale offset for Prox position only, in mils [0] 0 to 90	Difference Limit for Voted TMR Inputs in Volts or Mils [2] -100 to 100	Voltage difference from gap voltage where keyphasor triggers [2.0] 1.0 to 5.0
GAP13_KPH1	AnalogIn-put	REAL	Average Air Gap,DC component of input#10	Sensor Type, group 3 [Unused], PosProx, KeyPhasor				

KPH_Type	GnBiasOvr-ide	Snsr_Offset	Gain	SysLim1E-nabl	SysLim1-Latch	SysLim1Type	SysLimit1
[Slot], Pedestal	Gain Bias Override [Disable], Enable	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled [10] ±13.5	Resolution of input signal (net gain unchanged), select based on expected range, use only if GnBiasOvride is enabled [1x], ‡ 2x, 4x, ‡ 8x	Enable System Limit 1 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 1 Check Type [>=] , <=	System Limit 1 – GAP in negative volts (Velomitor) or positive mils (Prox) [90] -100 to 100

‡Gain 2x and Gain 8x are **Never** valid on GAP12_KPH2.

SysLim2Enabl	SysLim2Latch	SysLim2Type	SysLimit2
Enable System Limit 2 [Disable], Enable	Latch the alarm [Latch], NotLatch	System Limit 2 Check Type [>=] , <=	System Limit 2 – GAP in negative volts (Velomitor) or positive mils (Prox) [10] -100 to 100

5.6.4 YVIBS1A Configuration

YVIB Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex TMR
Hardware group		Distributed I/O Group
Main terminal board	Terminal board type/HW form/barcode/Group/TB Location	TVBA
I/O pack configurations	Pack form/TB Connector/IONet	

Parameters Tab

YVIB Parameter	Description	Choices
SystemLimits	Enable system limits	Enable Disable
Vib_PP_Fltr	First order filter time constant (sec)	0.04 to 2
MaxVolt_Prox	Maximum Input Volts (pk-neg), healthy Input, Prox	-4 to 0
MinVolt_Prox	Minimum Input Volts (pk-neg), healthy Input, Prox	-24 to -16
MaxVolt_KP	Maximum Input Volts (pk-neg), healthy Input, Keyphasor transducer	-4 to 0
MinVolt_KP	Minimum Input Volts (pk-neg), healthy Input, Keyphasor transducer	-24 to -16
MaxVolt_Seis	Maximum Input Volts (pk-pos), healthy Input, Seismic	0 to 2.5
MinVolt_Seis	Minimum Input Volts (pk-neg), healthy Input, Seismic	-2.5 to 0
MaxVolt_Acc	Maximum Input Volts (pk-neg), healthy Input, Accel	-12 to 1.5
MinVolt_Acc	Minimum Input Volts (pk-neg), healthy Input, Accel	-24 to -1
MaxVolt_Vel	Maximum Input Volts (pk-neg), healthy Input, Velomitor* sensors	-12 to 1.5
MinVolt_Vel	Maximum Input Volts (pk-neg), healthy Input, Velomitor sensors	-24 to -1

YVIB Variables	Description	Setting
LM_RPM_A	Speed A in RPM (calculated externally to the YVIB)	(Output FLOAT)
LM_RPM_B	Speed B in RPM (calculated externally to the YVIB)	(Output FLOAT)
LM_RPM_C	Speed C in RPM (calculated externally to the YVIB)	(Output FLOAT)

Vib 1-8 Configuration 1 Tab

Vib 1-8	Description	Setting
TMR_DiffLmt	Difference Limit for Voted TMR Inputs in V or Mils	-1200 to 1200
FilterType	Filter used for Velomitor sensors and Seismic only	None Low Pass High Pass Band Pass
Fltrhpcutoff	High Pass 3db point (cutoff in Hz)	4 to 30 Hz
Fltrhpattn	Slope or attenuation of filter after cutoff	2 pole 4 pole 6 pole 8 pole
Fltrlpcutoff	Low Pass 3db point (cutoff in Hz)	300 to 2300 Hz
Fltrhpattn	Slope or attenuation of filter after cutoff	2 pole 4 pole 6 pole 8 pole
SysLim1Enabl	Enable system limit 1 fault check	Disable Enable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 - check type (≥ or ≤)	≥ ≤
SysLimit1	System limit 1 - vibration in mils (Prox) or inch/sec (seismic, acel)	-1200 to 1200
SysLim2Enabl	Enable system limit 2 fault check	Disable Enable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 - check type (≥ or ≤)	≥ ≤
SysLimit2	System limit 2 - vibration in mils (Prox) or inch/sec (seismic, acel)	-1200 to 1200

Gap 1-3 Tab

Gap 1-3	Description	Setting
VIB_Type	Type of vibration probe	Unused PosProx VibProx VibProx-KPH VibLMAccel VibSeismic VibVelomitor
Scale	V/mil or V/ips	0 to 2
Scale_Off	Scale offset for Prox position only, in mils	0 to 1200
GnBiasOvride	Gain Bias Override	Enable Disable
Snsr_Offset	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled	±13.5 V dc
Gain	Used only when GnBiasOvride = Enables and modifies the resolution of the incoming signal	1x 2x 4x 8x
LMIpcutoff	Tracking filter lowpass cutoff frequency in Hz	1.5 2 2.5 3 3.5 4 4.5 5
TMR_DiffLmt	Difference Limit for Voted TMR Inputs in V or Mils	-1200 to 1200
SysLim1Enabl	Enable system limit 1 fault check	Disable Enable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 - check type (≥ or ≤)	≥ ≤
SysLimit1	System limit 1 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200
SysLim2Enabl	Enable system limit 2 fault check	Disable Enable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 - check type (≥ or ≤)	≥ ≤
SysLimit2	System limit 2 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200

Gap 4-8 Tab

Gap 4-8	Description	Setting
VIB_Type	Type of vibration probe	Unused PosProx VibProx VibProx-KPH VibSeismic VibVelomitor
Scale	V/mil or V/ips	0 to 2
Scale_Off	Scale offset for Prox position only, in mils	0 to 1200
GnBiasOvride	Gain Bias Override	Enable Disable
Snsr_Offset	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled	±13.5 V dc
Gain	Used only when GnBiasOvride = Enables and modifies the resolution of the incoming signal	1x 2x 4x 8x
TMR_DiffLmt	Difference Limit for Voted TMR Inputs in V or Mils	-1200 to 1200
SysLim1Enabl	Enable system limit 1 fault check	Disable Enable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 - check type (≥ or ≤)	≥ ≤
SysLimit1	System limit 1 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200
SysLim2Enabl	Enable system limit 2 fault check	Disable Enable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 - check type (≥ or ≤)	≥ ≤
SysLimit2	System limit 2 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200

Gap 9-12 Tab

Gap 9-12	Description	Setting
VIB_Type	Type of vibration probe	Unused PosProx
Scale	V/mil or V/ips	0 to 2
Scale_Off	Scale offset for Prox position only, in mils	0 to 1200
GnBiasOvride	Gain Bias Override	Enable Disable
Snsr_Offset	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled	±13.5 V dc
Gain	Used only when GnBiasOvride = Enables and modifies the resolution of the incoming signal	1x 4x
TMR_DiffLmt	Difference Limit for Voted TMR Inputs in V or Mils	-1200 to 1200
SysLim1Enabl	Enable system limit 1 fault check	Disable Enable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 - check type (≥ or ≤)	≥ ≤
SysLimit1	System limit 1 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200
SysLim2Enabl	Enable system limit 2 fault check	Disable Enable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 - check type (≥ or ≤)	≥ ≤
SysLimit2	System limit 2 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200

KPH Tab

KPH	Description	Setting
VIB_Type	Type of vibration probe	Unused PosProx KetPhasor
Scale	V/mil or V/ips	0 to 2
Scale_Off	Scale offset for Prox position only, in mils	0 to 1200
KPH_Thrshld	Sets voltage threshold point for pulse detect comparator	1 to 5
KPH_Type		Slot Pedestal
GnBiasOvride	Gain Bias Override	Enable Disable
Snsr_Offset	Amount of bias voltage (dc) to remove from input signal used to max. A/Ds signal range used only when GnBiasOvride is enabled	±13.5 V dc
Gain	Used only when GnBiasOvride = Enables and modifies the resolution of the incoming signal	1x 2x 4x 8x
TMR_DiffLmt	Difference Limit for Voted TMR Inputs in V or Mils	-1200 to 1200
SysLim1Enabl	Enable system limit 1 fault check	Disable Enable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 - check type (≥ or ≤)	≥ ≤
SysLimit1	System limit 1 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200
SysLim2Enabl	Enable system limit 2 fault check	Disable Enable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 - check type (≥ or ≤)	≥ ≤
SysLimit2	System limit 2 - gap in negative V (for Vel) or positive mils (for Prox)	-1200 to 1200

TVBA Jumper

TVBA Jumper	Select	
J1A	Seismic (S)	
	Prox or Accel (P, A)	
	Velomitor sensors (V)	
J2A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J3A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J4A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J5A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J6A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J7A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	
J8A	Seismic (S) Prox or Accel (P, A) Velomitor sensors (V)	

TVBA Jumper	Select	
J1B	Seismic (S)	
	Prox, Velomitor sensors or Accel (P, V, A)	
J2B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J3B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J4B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J5B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J6B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J7B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	
J8B	Seismic (S) Prox, Velomitor sensors or Accel (P, V, A)	

TVBA Jumper	Select
J1C	PCOM OPEN
J2C	PCOM OPEN
J3C	PCOM OPEN
J4C	PCOM OPEN
J5C	PCOM OPEN
J6C	PCOM OPEN
J7C	PCOM OPEN
J8C	PCOM OPEN

5.7 YPRO

YPRO Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex TMR
Hardware group		Distributed I/O Group
Main terminal board	Terminal board type/HW form/barcode/Group/TB Location	SPRO TPRO
Auxiliary terminal Board	Terminal board Phy Pos/type/HW form/Group/TB Location	TREG
I/O pack configurations	Pack form/TB Connector/IONet	S1B

Parameters Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
TurbineType	Turbine type and trip solenoid configuration	Unused GT_1Shaft LM_3Shaft MediumSteam SmallSteam GT_2Shaft Stag_GT_1Sh Stag_GT_2Sh LargeSteam LM_2Shaft
LMTripZEnabl	On LM machine, when no PR on Z, enable a vote for trip	Disable Enable
TA_Trp_Enab1	Steam, enable trip anticipate on ETR1	Disable Enable
TA_Trp_Enab2	Steam, enable trip anticipate on ETR2	Disable Enable
TA_Trp_Enab3	Steam, enable trip anticipate on ETR3	Disable Enable
SpeedDifEn	Enable trip on speed difference between controller and YPRO	Disable Enable
StaleSpdEn	Enable trip on speed from controller freezing	Disable Enable
RotateLeds	Rotate the status LEDs if all status are OK	Disable Enable
LedDiags	Generate diagnostic alarm when LED status lit	Disable Enable
RatedRPM_TA	Rated RPM, used for trip anticipator and for speed diff protection	
SilMode	Perform additional SIL diagnostic and trip checks	Disable, Enable

Parameters Tab (continued)

YPRO Parameter	Description	Select Option ✓ or Enter Value
AccelCalType	Select acceleration calculation time (ms)	
OS_Diff	Absolute speed difference in percent for trip threshold	

Pulse Rate Tab (3 each)

YPRO Pulse Rates	Description	Select Option ✓ or Enter Value
PRType	Pulse rate type	Unused Flow Speed Speed High Speed LM
PRScale	Pulses per revolution	0 to 1000
OSHW_Setpoint	Hardware overspeed trip set point in RPM	0 to 20000
OS_Setpoint	Overspeed trip set point in RPM	0 to 20000
OS_Tst_Delta	Offline overspeed test set point delta in RPM	-2000 to 2000
Zero_Speed	Zero speed for this shaft in RPM	0 to 20000
Min_Speed	Minimum speed for this shaft in RPM	0 to 20000
Accel_Trip	Enable acceleration trip	Enable Disable
Acc_Setpoint	Acceleration trip set point in RPM	0 to 20000
TMR_DiffLimit	Diagnostic limit, TMR vote difference limit in engineering units	0 to 20000

PT Input Tab (BUS and GEN)

YPRO Parameter	Description	Select Option ✓ or Enter Value
PT_Input	PT primary in engineering nits (kv or percent) for PT_ Output	1 to 1000
PT_Output	PT output in volts rms for PT_Input – typically 115	0 to 150
TMR_DiffLimt	Diag Limit, TMR input vote difference, in engineering units	1 to 1000

E-stop (SPRO) Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable

E-stop Tab (TREA)

YPRO Parameter	Description	Select Option ✓ or Enter Value
EstopEnab	Enable E-stop detection on TREA board	Disable Enable
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable

ETR Relays Tab (3 TREG, 2 TREA)

YPRO Parameter	Description	Select Option ✓ or Enter Value
RelayOutput	Relay signal	Unused Used
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable
DiagSolEnab	Enable solenoid voltage diagnostic	Disable Enable

K25 Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
SynchCheck	Synch check relay K25A used	Unused Used
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable
SystemFreq	System frequency in hertz	60 Hz 50 Hz
ReferFreq	Select freq reference for PLL, PR_Std input (If single shaft PR1, otherwise PR2) or from signal space	PR_Std SgSpace
TurbRPM	Rated RPM, load turbine	0 to 20000
VoltageDiff	Maximum voltage diff in engineering nits (kv or percent) for synchronizing	1 to 1000
FreqDiff	Maximum frequency difference in hertz for synchronizing	0 to 0.5
PhaseDiff	Maximum phase difference in degrees for synchronizing	0 to 30
GenVoltage	Allowable minimum generator voltage, engineering units (kv or percent) for synchronizing. Typically 50% of rated	1 to 1000
BusVoltage	Allowable minimum bus voltage, engineering units (kv or percent) for synchronizing. Typically 50% of rated	1 to 1000

K4CL Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
Signal	Relay signal	Unused Used
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable

Econ Relays (3) Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
Signal	Relay signal	Unused Used
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable

Contacts (7) Tab

YPRO Parameter	Description	Select Option ✓ or Enter Value
ContactInput	Contact input	Unused Used
SeqOfEvents	Record contact transitions in sequence of events	Disable Enable
DiagVoteEnab	Enable voting disagreement diagnostic	Disable Enable
TripMode	Trip mode	Direct Conditional Disable

TREA

YPRO Speed Input Connections	Function	Jumper
Wire to all 9 pulse inputs: PR1_X – PR3_Z	Each set of three pulse inputs goes to its own dedicated YPRO I/O pack.	Cannot use jumper: Place in STORE position.
Wire to bottom 3 pulse inputs only: PR1_X – PR3_X; No wiring to PR1_Y-PR3_Z	The same set of signals is fanned to all the YPRO I/O packs.	Use jumper: Place over pin pairs.

TREA Jumper

YPRO Jumper	Select ✓
P1	FAN STORE
P2	FAN STORE

5.8 YSIL

5.8.1 YSIL Configuration

5.8.1.1 Parameters

Default values are in blue.

Name	Value	Description
PRGrouping	2Shafts_3Sensors 3Shafts_2Sensors 3Shafts_3Sensors	Select grouping of speed inputs: 2 Shafts (3 speed sensors/shaft), 3 shafts (2 speed sensors/shaft), 3 shafts (3 speed sensors/shaft)
LMTripZEnabl	Enable Disable	On LM machine,when no PR on Z, Enable a vote for Trip
TA_Trp_Enab1	Enable Disable	Steam, Enable Trip Anticipate on ETR1
TA_Trp_Enab2	Enable Disable	Steam, Enable Trip Anticipate on ETR2
TA_Trp_Enab3	Enable Disable	Steam, Enable Trip Anticipate on ETR3
SpeedDifEn	Enable Disable	Enable Trip on Speed Difference between Controller & YSIL
StaleSpdEn	Enable Disable	Enable Trip on Speed from Controller Freezing
No_T_PS_Req	Enable Disable	No Flame Detect Power Supply required for T
RotateLeds	Enable Disable	Rotate the Status LEDs if all status are OK
LedDiags	Enable Disable	Generate diag alarm when LED status lit
TurbineType	Unused GT_1Shaft GT_2Shaft LargeSteam LM_2Shaft LM_3Shaft MediumSteam SmallSteam Stag_GT_1Sh Stag_GT_2Sh	Turbine Type and Trip Solenoid Configuration
RatedRPM_TA	3600 is default	Rated RPM, used for Trip Anticipater and for Speed Diff Protection
AccelCalType	70 is default	Select Acceleration Calculation Time (msec)
OS_Diff	5.0 is default	Absolute Speed Difference in Percent For Trip Threshold
AMS_Mux_Scans_Permitted	Enable Disable	AMS mulitplexer scans for command 1 and 2 are allowed (command 3 always allowed). Refer to the section, *Asset Management System Tunnel Command* for more information.
Min_MA_Input	3.8 is default	Minimum mA for Healthy 4–20 mA Input

Name	Value	Description
Max_MA_Input	20.5 is default	Maximum mA for Healthy 4–20 mA Input
Excitation_Volt	125V 24V 48V	Contact Input Excitation (wetting) Voltage (SCSA and TCSA must use the same voltage level)
TemperatureUnits	°C °F	Used for SCSA Thermocouples and Cold Junctions
SystemFreq	50Hz 60Hz	System frequency in Hz

5.8.1.2 Variables

Name	Direction	Data Type	Variable Description
L3DIAG_YSIL_R, S, or T	Input	BOOL	I/O Diagnostic Indication
LINK_OK_YSIL_R, S, or T	Input	BOOL	I/O Link Okay Indication
ATTN_YSIL_R, S, or T	Input	BOOL	I/O Attention Indication
PS18V_YSIL_R, S, or T	Input	BOOL	I/O 18V Power Supply Indication
PS28V_YSIL_R, S, or T	Input	BOOL	I/O 28V Power Supply Indication
SCSA_Comm_Status_R, S, or T	Input	BOOL	SCSA Serial Communication Status
L3SS_Comm	Input	BOOL	Controller Communication Status
GT_1Shaft	Input	BOOL	Config – Gas Turb,1 Shaft Enabled
GT_2Shaft	Input	BOOL	Config – Gas Turb,2 Shaft Enabled
LM_2Shaft	Input	BOOL	Config – LM Turb,2 Shaft Enabled
LM_3Shaft	Input	BOOL	Config – LM Turb,3 Shaft Enabled
LargeSteam	Input	BOOL	Config – Large Steam, Enabled
MediumSteam	Input	BOOL	Config – Medium Steam Enabled
SmallSteam	Input	BOOL	Config – Small Steam Enabled
Stage_GT_1Sh	Input	BOOL	Config – Stage 1 Shaft, Enabled
Stage_GT_2Sh	Input	BOOL	Config – Stage 2 Shaft, Enabled
IOPackTmpr_R, S, or T	AnalogInput	REAL	IO Pack Temperature (deg F)
LockedRotorByp	Output	BOOL	LL97LR_BYP - Locked Rotor Bypass
HPZeroSpdByp	Output	BOOL	L97ZSC_BYP - HP Zero Speed Check Bypass
DriveFreq	AnalogOutput	REAL	RefrFreq - Drive (Gen) Freq (Hz), used for non standard drive config Can be used for zero speed logic in Dead Bus Closure of breaker
Speed1	AnalogOutput	REAL	Shaft Speed 1 in RPM
ControllerWdog	Output	DINT	Controller Watchdog Counter
CJBackup_R, S, or T	AnalogOutput	REAL	CJ Backup Value °C/°F Based on configured TemperatureUnits
CJRemote_R, S, or T	AnalogOutput	REAL	CJ Remote Value °C/°F Based on configured TemperatureUnits
TA_StptLoss	Input	BOOL	(L30TA) True if Trip Anticipate overspeed setpoint from TR_Spd_Sp is too far from rated RPM RatedRPM_TA

5.8.1.3 Vars-AI Trip

Name	Direction	Data Type	Vars-AI Description
AnalogInput01_Trip_R, S, or T	Input	BOOL	SCSA Analog Input Trip Status
↓			
AnalogInput16_Trip_R, S, or T	Input	BOOL	SCSA Analog Input Trip Status

5.8.1.4 Vars-Trip

Name	Direction	Data Type	Vars-Trip Description
WatchDog_Trip	Input	BOOL	Enhanced diag - Watch Dog trip
StaleSpeed_Trip	Input	BOOL	Enhanced diag - Stale Speed trip
SpeedDiff_Trip	Input	BOOL	Enhanced diag - Speed Difference trip
FrameMon_Flt	Input	BOOL	Enhanced diag - Frame Monitor Fault
OverSpd1_Trip	Input	BOOL	L12HP_TP - HP overspeed trip
OverSpd2_Trip	Input	BOOL	L12LP_TP - LP overspeed trip
OverSpd3_Trip	Input	BOOL	L12IP_TP - IP overspeed trip
Decel1_Trip	Input	BOOL	L12HP_DEC - HP de-acceleration trip
Decel2_Trip	Input	BOOL	L12LP_DEC - LP de-acceleration trip
Decel3_Trip	Input	BOOL	L12IP_DEC - IP de-acceleration trip
Accel1_Trip	Input	BOOL	L12HP_ACC - HP acceleration trip
Accel2_Trip	Input	BOOL	L12LP_ACC - LP acceleration trip
Accel3_Trip	Input	BOOL	L12IP_ACC - IP acceleration trip
HW_OverSpd1_Trip	Input	BOOL	L12HP_HTP - HP Hardware detected overspeed trip
HW_OverSpd2_Trip	Input	BOOL	L12LP_HTP - LP Hardware detected overspeed trip
HW_OverSpd3_Trip	Input	BOOL	L12IP_HTP - IP Hardware detected overspeed trip
TA_Trip	Input	BOOL	Trip Anticipate Trip,L12TA_TP
TSCA_Contact01_Trip	Input	BOOL	Contact Trip (L5Cont01_Trip)
↓			
TSCA_Contact20_Trip	Input	BOOL	Contact Trip (L5Cont20_Trip)
LPShaftLock	Input	BOOL	LP Shaft Locked
PR1_Zero	Input	BOOL	L14HP_ZE - HP shaft at zero speed
PR2_Zero	Input	BOOL	L14LP_ZE - LP shaft at zero speed
PR3_Zero	Input	BOOL	L14IP_ZE - IP shaft at zero speed
CompositeAnalog_Trip	Input	BOOL	Composite Analog Trip Status
CompositeTrip	Input	BOOL	Composite Trip Status
Estop_Trip	Input	BOOL	ESTOP Trip (L5ESTOP1)
Config1_Trip	Input	BOOL	HP Config Trip(L5CFG1_Trip)
Config2_Trip	Input	BOOL	LP Config Trip(L5CFG2_Trip)

Name	Direction	Data Type	Vars-Trip Description
Config3_Trip	Input	BOOL	IP Config Trip(L5CFG3_Trip)
Cross_Trip	Output	BOOL	L4Z_XTRP - Control Cross Trip

5.8.1.5 Vars-Flame

Name	Direction	Data Type	Vars-Flame Description
FlameDetPwrStat	Input	BOOL	335 V dc status
FD1_Flame	Input	BOOL	Flame Detect present
↓			
FD8_Flame	Input	BOOL	Flame Detect present
FD1_Level	Output	BOOL	1 = High Detection Cnts Level
↓			
FD8_Level	Output	BOOL	1 = High Detection Cnts Level

5.8.1.6 Vars-Contacts

Name	Direction	Data Type	Description
TCSA_Contact01_TripEnab	Input	BOOL	Config – Contact Trip Enabled – Direct
↓			
TCSA_Contact20_TripEnab			

5.8.1.7 Vars-Speed

Name	Direction	Data Type	Vars-Speed Description
Accel1_TrEnab	Input	BOOL	Config – Accel 1 Trip Enabled
Accel2_TrEnab	Input	BOOL	Config – Accel 2 Trip Enabled
Accel3_TrEnab	Input	BOOL	Config – Accel 3 Trip Enabled
HW_OverSpd1_Setpt_Pend	Input	BOOL	Hardware HP overspeed setpoint changed after power up
HW_OverSpd2_Setpt_Pend	Input	BOOL	Hardware LP overspeed setpoint changed after power up
HW_OverSpd3_Setpt_Pend	Input	BOOL	Hardware IP overspeed setpoint changed after power up
HW_OverSpd1_Setpt_CfgErr	Input	BOOL	Hardware HP Overspd Setpoint Config Mismatch Error
HW_OverSpd2_Setpt_CfgErr	Input	BOOL	Hardware LP Overspd Setpoint Config Mismatch Error
HW_OverSpd3_Setpt_CfgErr	Input	BOOL	Hardware IP Overspd Setpoint Config Mismatch Error
OverSpd1_Setpt_CfgErr	Input	BOOL	HP Overspd Setpoint Config Mismatch Error
OverSpd2_Setpt_CfgErr	Input	BOOL	LP Overspd Setpoint Config Mismatch Error
OverSpd3_Setpt_CfgErr	Input	BOOL	IP Overspd Setpoint Config Mismatch Error
PR1_Accel	AnalogInput	REAL	HP Accel in RPM/SEC
PR2_Accel	AnalogInput	REAL	LP Accel in RPM/SEC

Name	Direction	Data Type	Vars-Speed Description
PR3_Accel	AnalogInput	REAL	IP Accel in RPM/SEC
PR1_Max	AnalogInput	REAL	HP Max Speed since last Zero Speed in RPM
PR2_Max	AnalogInput	REAL	LP Max Speed since last Zero Speed in RPM
PR3_Max	AnalogInput	REAL	IP Max Speed since last Zero Speed in RPM
PR1_Spd	AnalogInput	REAL	PR1 - Speed sensor 1 (1A if three or two groups, see PRGrouping parameter)
PR2_Spd	AnalogInput	REAL	PR2 - Speed sensor 2 (2A if three groups, 1B if two groups, see PRGrouping parameter)
PR3_Spd	AnalogInput	REAL	PR3 - Speed sensor 3 (3A if three groups, 2A if two groups, see PRGrouping parameter)
PR4_Spd	AnalogInput	REAL	PR4 - Speed sensor 4 (1B if three groups, 1C if two groups, see PRGrouping parameter)
PR5_Spd	AnalogInput	REAL	PR5 - Speed sensor 5 (2B if three or two groups, see PRGrouping parameter)
PR6_Spd	AnalogInput	REAL	PR6 - Speed sensor 6 (3B if three groups, 2C if two groups, see PRGrouping parameter)
OverSpd1_Test_OnLine	Output	BOOL	L97HP_TST1 - OnLine HP Overspeed Test
OverSpd2_Test_OnLine	Output	BOOL	L97LP_TST1 - OnLine LP Overspeed Test
OverSpd3_Test_OnLine	Output	BOOL	L97IP_TST1 - OnLine IP Overspeed Test
OverSpd1_Test_OffLine	Output	BOOL	L97HP_TST2 - OffLine HP Overspeed Test
OverSpd2_Test_OffLine	Output	BOOL	L97LP_TST2 - OffLine LP Overspeed Test
OverSpd3_Test_OffLine	Output	BOOL	L97IP_TST2 - OffLine IP Overspeed Test
TripAnticipateTest	Output	BOOL	L97A_TST - Trip Anticipate Test
PR_Max_Reset	Output	BOOL	Max Speed Reset
OnLineOverSpd1X	Output	BOOL	L43EOST_ONL - On Line HP Overspeed Test,with auto reset
OverSpd1_Setpt	AnalogOutput	REAL	HP Overspeed Setpoint in RPM
OverSpd2_Setpt	AnalogOutput	REAL	LP Overspeed Setpoint in RPM
OverSpd3_Setpt	AnalogOutput	REAL	IP Overspeed Setpoint in RPM
OverSpd1_TATrip_Setpt	AnalogOutput	REAL	PR1 Overspeed Trip Setpoint in RPM for Trip Anticipate Fn
HWOverSpd_Setpt1	AnalogOutput	REAL	HP Hardware Overspeed Setpoint in RPM
HWOverSpd_Setpt2	AnalogOutput	REAL	LP Hardware Overspeed Setpoint in RPM
HWOverSpd_Setpt3	AnalogOutput	REAL	IP Hardware Overspeed Setpoint in RPM
Repeater1	Input	BOOL	Speed Repeater Fault Status
↓			
Repeater6	Input	BOOL	Speed Repeater Fault Status

5.8.1.8 Vars-Relay

The following are the contact feedbacks for the electromechanical safety relays. They must be closed (feedback True) for current to flow in the ETRs.

Contact Feedbacks

Name	Direction	Data Type	Description
Mech1_Fdbk	Input	BOOL	Mechanical relay feedback, controls group 1 (K1–3)
Mech2_Fdbk	Input	BOOL	Mechanical relay feedback, controls group 2 (K4–6)
Mech3_Fdbk	Input	BOOL	Mechanical relay feedback, controls group 3 (K7–9)

The following are the Output Bits, which can be used to open ETR Relays. They are only available when the ETRs are configured as *Used* and TripMode configuration as *Enable* (from the *ETR Relay* tab).

Output Bits

Name	Direction	Data Type	Description
ETR1_Open	Output	BOOL	ETR1 Open Command, True de-energizes relay
ETR2_Open	Output	BOOL	ETR2 Open Command, True de-energizes relay
ETR3_Open	Output	BOOL	ETR3 Open Command, True de-energizes relay
ETR4_Open	Output	BOOL	ETR4 Open Command, True de-energizes relay
ETR5_Open	Output	BOOL	ETR5 Open Command, True de-energizes relay
ETR6_Open	Output	BOOL	ETR6 Open Command, True de-energizes relay
ETR7_Open	Output	BOOL	ETR7 Open Command, True de-energizes relay
ETR8_Open	Output	BOOL	ETR8 Open Command, True de-energizes relay
ETR9_Open	Output	BOOL	ETR9 Open Command, True de-energizes relay

Note When the relay outputs are configured as *TripMode* **Disable**, the associated mechanical relay will pick up when any of the three solid state relays pick up within that group, and drops when all the solid state relays are False in that group.

5.8.1.9 Vars-Sync

Name	Direction	Data Type	Vars-Sync Description
GenFreq	AnalogInput	REAL	DF2 hz
BusFreq	AnalogInput	REAL	SFL2 hz
GenVoltsDiff	AnalogInput	REAL	DV_ERR KiloVolts rms - Gen Low is Negative
GenFreqDiff	AnalogInput	REAL	SFDIFF2 Slip hz - Gen Slow is Negative
GenPhaseDiff	AnalogInput	REAL	SSDIFF2 Phase degrees - Gen Lag is Negative
SyncCheck_Enab	Output	BOOL	L25A_PERM - Sync Check Permissive
SyncCheck_ByPass	Output	BOOL	L25A_BYPASS - Sync Check ByPass Used for dead bus breaker closure feature

5.8.1.10 TSCA Contacts

Default values are in blue.

Name	Direction	Data Type	Description	ContactInput	SeqOfEvents	DiagVoteEnab	TripMode
TCSA_Contact01	Input	BOOL	Contact Input 1	Used Unused	Enable Disable	Enable Disable	Disable Enable
↓			↓				
TCSA_Contact20			Contact Input 20				

5.8.1.11 EStop

Default values are in blue.

Name	Direction	Data Type	Description	DiagVoteEnab
ESTOP_Fdbk	Input	BOOL	ESTOP, inverse sense, True = Run	Enable Disable

5.8.1.12 ETR Relay

Default values are in blue.

Name	Direction	Data Type	Description	RelayOutput	TripMode †
K4	Output	BOOL	K4 Relay Ouput, Emergency Trip Relay when Trip Mode Enabled	Used Unused	Enable Disable ‡
K5	Output	BOOL	K5 Relay Ouput, Emergency Trip Relay when K4 Trip Mode Enabled		N/A
K6	Output	BOOL	K6 Relay Ouput, Emergency Trip Relay when K4 Trip Mode Enabled		N/A
K7	Output	BOOL	K7 Relay Ouput, Emergency Trip Relay when Trip Mode Enabled		Enable Disable ‡
K8	Output	BOOL	K8 Relay Ouput, Emergency Trip Relay when K7 Trip Mode Enabled		N/A
K9	Output	BOOL	K9 Relay Ouput, Emergency Trip Relay when K7 Trip Mode Enabled		N/A

Note † TripMode on ETR Relay can only be selected in groups. K4-K6 are in one group, and K7-K9 are in another group.

Note ‡ When the relay outputs are configured as TripMode **Disable**, the associated mechanical relay will pick up when any of the three solid state relays pick up within that group, and drops when all the solid state relays are False in that group.

5.8.1.13 ETR Fdbk

Default values are in blue.

Name	Direction	Data Type	Description	SeqOfEvents	DiagVoteEnab
K1_Fdbk	Input	BOOL	Trip Relay Feedback	Enable Disable	Enable Disable
K2_Fdbk	Input	BOOL	Trip Relay Feedback		
K3_Fdbk	Input	BOOL	Trip Relay Feedback		
K4_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		
K5_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		
K6_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		
K7_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		
K8_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		
K9_Fdbk	Input	BOOL	Normal / Trip Relay Feedback		

5.8.1.14 TSCA Relay

Default values are in blue.

Name	Direction	Data Type	Description	RelayOutput	Output_State	Output_Value
TCSA_Relay01	Output	BOOL	Under control of SyncCheck if SyncCheck is configured for Relay01	Used Unused	HoldLastVal Output_Value PwrDownMode	On Off
TCSA_Relay02	Output	BOOL	Under control of SyncCheck if SyncCheck is configured for Relay02			

5.8.1.15 TCSA Relay Fdbk

Default values are in blue.

Name	Direction	Data Type	Description	SeqOfEvents	DiagVoteEnab
TCSA_Relay01Fdbk	Input	BOOL	Relay Feedback	Enable Disable	Enable Disable
TCSA_Relay02Fdbk	Input	BOOL	Relay Feedback		

5.8.1.16 K25A

Default values are in blue.

Name	Direction	Data Type	Description	SynchCheck	DiagVoteEnab
K25A_Cmd_Status	Input	BOOL	Synch Check Relay	Relay01 Relay02 Unused	Disable Enable

GenFreqSource	TurbRPM	VoltageDiff	FreqDiff	PhaseDiff	GenVoltage	BusVoltage
PR_Std SgSpace	Default is 3600	Default is 2.8	Default is 0.30	Default is 10.0	Default is 6.9	Default is 6.9

5.8.1.17 Pulse Rate

Default values are in blue.

Name	Direction	Data Type	Description	PRType	PRScale	HwOverSpd_Setpt	OverSpd_Setpt
PulseRate1	AnalogInput	REAL	HP speed	Unused Speed Speed_High Speed_LM	Default is 60	Default is 0	Default is 0
PulseRate2	AnalogInput	REAL	LP speed				
PulseRate3	AnalogInput	REAL	IP speed				

OverSpd_Test_Delta	Zero_Speed	Min_Speed	Accel_Trip	Accel_Setpt	TMR_DiffLimt	Dual_DiffLimit
Default is 0	Default is 0	Default is 0	Enable Disable	Default is 0	Default is 5	Default is 25

5.8.1.18 PT Inputs

The following PT inputs on the TCSA are fanned, single phase (75 to 130 V rms).

Name	Direction	Data Type	Description	PT_Input	PT_Output	TMR_DiffLimt
GenPT_KVolts	AnalogInput	REAL	Kilo-Volts RMS (Active only if K25A is Enabled)	Default is 13.8	Default is 115	Default is 1
BusPT_KVolts	AnalogInput	REAL	Kilo-Volts RMS (Active only if K25A is Enabled)			

5.8.1.19 TCSA Analog Inputs

Default values are in blue.

Name	Direction	Data Type	Description	Input	Low_Input	Low_Value
FlameAnalogInput01	AnalogInput	REAL	Flame Analog Input	Used Unused	Default is 4	Default is 0
↓						
FlameAnalogInput10						

High_Input	High_Value	InputFilter	DiagHighEnab	DiagLowEnab	TMR_DiffLimt
Default is 20	Default is 100	Used Unused	Enable Disable	Enable Disable	Default is 5

5.8.1.20 Flame

Name	Direction	Data Type	Description	FlmDetTime
FlameInd1	AnalogInput	REAL	Flame Intensity (Hz)	0.040sec 0.080sec 0.160sec
↓				
FlameInd8				

FlameLimitHi	FlameLimitLow	Flame_Det	TMR_DiffLimt
Default is 5	Default is 3	Used Unused	Default is 5

5.8.1.21 SCSA Analog Inputs

Default values are in blue.

Name	Data Type	Description	Input	Low_Input	Low_Value	High_Input	High_Value	InputFilter
AnalogInput01_ R, S, or T	REAL	4–20 mA	4–20ma Unused	Default is 4	Default is 0	Default is 20	Default is 100	0.75hz 1.5hz 3hz 6hz 12hz Unused
↓								
AnalogInput16_ R, S, or T	REAL	4–20 mA		Default is 4	Default is 0	Default is 20	Default is 100	

DiagHighEnab DiagLowEnab	TripEnab	TripSetPoint	TripDelay	HART_Enable	HART_MfgID HART_DevType HART_DevID
Enable Disable	Enable Disable	Default is 0	Default is 100 (milliseconds)	Enable Disable	Default is 0

5.8.1.22 SCSA Thermocouple Inputs

Default values are in blue.

Name	Type	ReportOpenTC
Thermocouple01_R, S, or T Thermocouple02_R, S, or T Thermocouple03_R, S, or T	Unused Type_J Type_K Type_S Type_T Type_E mV	Fail_Hot Fail_Cold *ReportOpenTC sets the failed state of an open thermocouple to either hot (high) or cold (low). This does not apply when Type = mV.*

5.8.1.23 SCSA Cold Junction

Default values are in blue.

Name	Direction	Data Type	Description	ColdJuncType
ColdJunction_R, S, or T	AnalogInput	REAL	Cold Junction for TCs 1 to 3	Local Remote

5.8.1.24 SCSA Relay

Default values are in blue.

Name	Direction	Data Type	RelayOutput	Output_State	Output_Value
SCSA_Relay01_R, S, or T	Output	BOOL	Used Unused	HoldLastVal Output_Value PwrDownMode	On Off
SCSA_Relay02_R, S, or T	Output	BOOL			

5.8.1.25 SCSA Relay Fdbk

Name	Direction	Data Type	Description
SCSA_Relay01Fdbk_R, S, or T	Input	BOOL	Relay Feedback
SCSA_Relay02Fdbk_R, S, or T	Input	BOOL	Relay Feedback

5.8.1.26 SCSA Contacts

Default values are in blue.

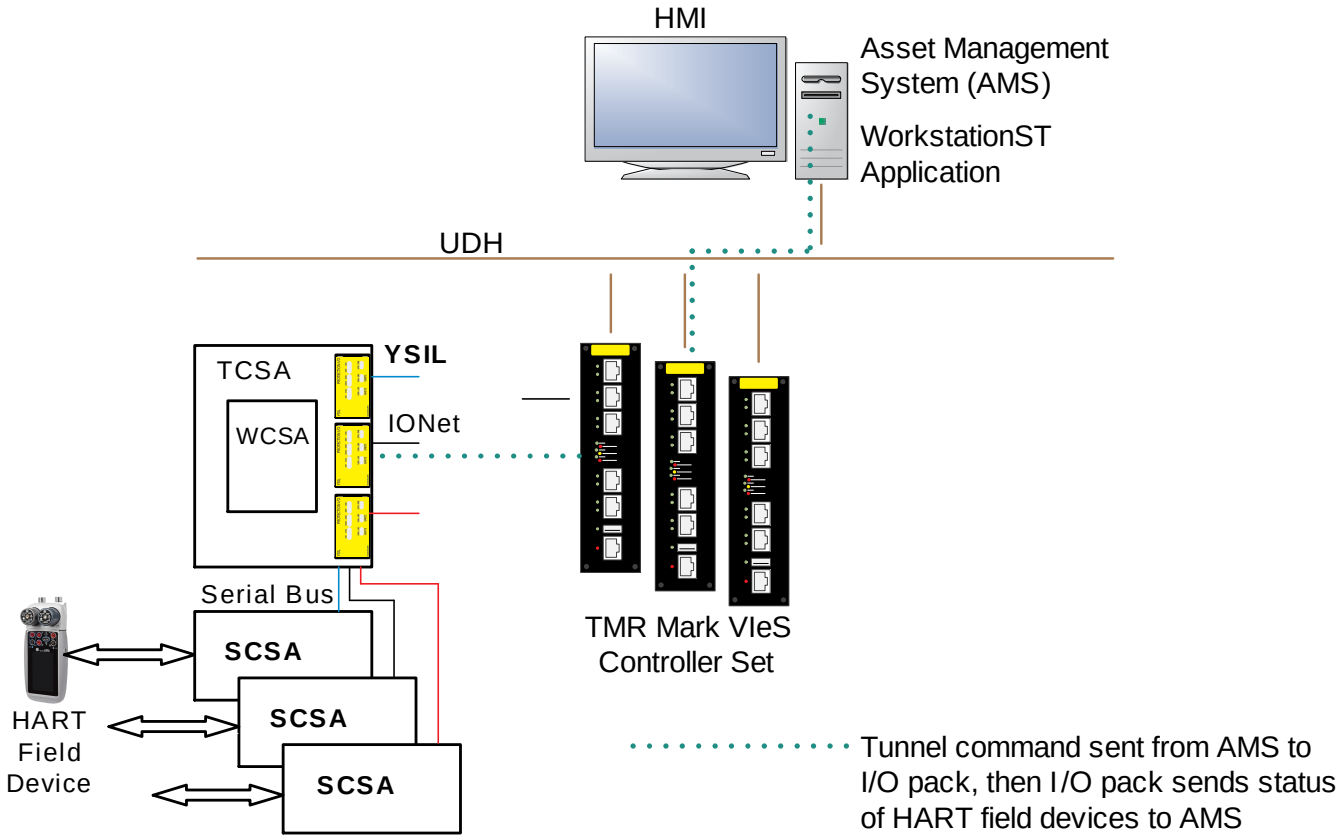
Name	Direction	Data Type	Description	ContactInput	SignalInvert	SignalFilter
SCSA_Contact01_R, S, or T	Input	BOOL	Contact Input	Used Unused	Invert Normal	100ms 10ms 20ms 50ms Unfiltered
↓						
SCSA_Contact03_R, S, or T	Input	BOOL	Contact Input			

5.8.2 Asset Management System Tunnel Command

The Asset Management System (AMS) scans the HART-enabled field devices to determine health. This scan command decision is made in the AMS (not the I/O pack). The AMS can send scan commands over channels 1, 2, or 3. The YSIL I/O pack (or if using PHRA/YHRA) can be configured to either only allow for the scan command to occur on the default channel 3 or it can allow these scan commands to occur on any of the three channels (as determined by the AMS). By changing the parameter, *AMS_Mux_Scans_Permitted* to **Enable** (it is disabled by default), the I/O pack will accept a change from channel 3 (which is the default channel).

From the perspective of the AMS, the multiplexer is the I/O pack (YSIL, YHRA, or PHRA). † In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line.

Note † Retrieved Nov 13, 2014 from http://en.wikipedia.org/wiki/Multiplexer



Example of YSIL HART Communications

5.9 YTUR

YTUR Module

Configuration	Description	Select Option ✓ or Enter Value
I/O pack redundancy		Simplex TMR
Hardware group		Distributed I/O Group
Main terminal board	Terminal board type/HW form/barcode/Group/TB Location	TTUR TRPA
Auxiliary terminal board	Terminal board Phy Pos/type/HW form/Group/TB Location	TRPG TRPA
I/O pack configurations	Pack form/TB Connector/IONet	

Parameters Tab

YTUR Parameter	Description	Select Option ✓ or Enter Value
SystemLimits	Enable or disable all system limit checking	Enable Disable
SMredundancy	Used to determine how shaft monitor testing is controlled if a TMR application	Simplex TMR
AccelCalType	Select acceleration calculation type	10 to 100
TripType	Select fast trip algorithm	Unused PR_Single PR_Max
Trip Type (PR_Single)		
AccASetpoint	Acceleration Trip Setpoint, Chan A, RPM/Sec	0 to 1500
AccAEnable	Acceleration Trip Enable, Chan A	Enable Disable
AccBSetpoint	Acceleration Trip Setpoint, Chan B, RPM/sec	0 to 1500
AccBEnable	Acceleration Trip Enable, Chan B	Enable Disable
PR1Setpoint	Fast overspeed trip #1, set point, PR1, RPM	0 to 20000
PR1TrEnable	Fast overspeed trip #1, enable	Disable Enable
PR2Setpoint	Fast overspeed trip #2, set point, PR1, RPM	0 to 20000
PR2TrEnable	Fast overspeed trip #2, enable	Disable Enable
PR3Setpoint	Fast overspeed trip #3, set point, PR1, RPM	0 to 20000
PR3TrEnable	Fast overspeed trip #3, enable	Disable Enable
PR4Setpoint	Fast overspeed trip #4, set point, PR1, RPM	0 to 20000

Parameters Tab (continued)

YTUR Parameter	Description	Select Option ✓ or Enter Value
PR4TrEnable	Fast overspeed trip #4, enable	Disable Enable
InForChanA	Input change selection for Accel/Decel trip	Accel1 Accel2 Accel3 Accel4
InForChanB	Input change selection for Accel/Decel trip	Accel1 Accel2 Accel3 Accel4
Trip Type (PR_Max)		
InForChanA	Input change selection for Accel/Decel trip	Accel1 Accel2 Accel3 Accel4
InForChanB	Input change selection for Accel/Decel trip	Accel1 Accel2 Accel3 Accel4
AccelCalType	Select acceleration calculation type	10 to 100
DecelStpt	Deceleration set point, RPM/sec	0 to 1500 (FLOAT)
DecelEnab	Deceleration enable	Disable Enable
FastOS1Stpt	Fast overspeed trip #1 set point, max (PR1,PR2), RPM	0 to 20000 (FLOAT)
FastOS1Enabl	Fast overspeed trip #1, enable	Disable Enable
FastOS2Stpt	Fast overspeed trip #2 set point, max (PR3,PR4), RPM	0 to 20000 (FLOAT)
FastOS2Enabl	Fast overspeed trip #2, enable	Disable Enable
DiffSetpoint	DiffSetpoint	0 to 20000 (FLOAT)
DiffEnable	Difference speed trip, enable	Disable Enable

Flame Tab

YTUR Flame Detector	Description	Select Option ✓ or Enter Value
FlmDetTime	Flame detector time interval (seconds)	0.040 sec 0.080 sec 0.160 sec
FlameLimitHI	Flame threshold LimitHI (HI detection cnts means Low sensitivity)	0 to 160
FlameLimitLow	Flame threshold LimitHI (LOW detection cnts means high sensitivity)	0 to 160

Flame Tab (continued)

YTUR Flame Detector	Description	Select Option ✓ or Enter Value
Flame_Det	Flame detector used/unused	Used Unused
TMR_DiffLimit	Diag Limit, TMR input difference limit, in Hz	0 to 160

Pulse Rate Tab (4 each)

YTUR Pulse Rate	Description	Choices
PRType	Selects the type of pulse rate input, n (for proper resolution)	Unused Flow Speed Speed_High Speed_LM
PRScale	Pulses per revolution (outputs RPM)	0 to 1,000
SysLim1Enabl	Enable system limit 1 fault check	Enable Disable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 check type (= or =)	= =
SysLimit1	System limit 1 – RPM	0 to 20,000
SysLim2Enabl	Enable system limit 2 fault check (as above)	Enable Disable
SysLim2Latch	Latch system limit 2 fault	Latch Not Latch
SysLim2Type	System limit 2 check type (= or =)	= =
SysLimit2	System limit 2 – RPM	0 to 20,000
TMR_DiffLimit	Diag Limit, TMR input vote difference, in engineering units	0 to 20,000

Shunt V Tab

YTUR Shaft Voltage Monitor	Description	Select Option ✓ or Enter Value
SysLim1Enabl	Enable system limit 1	Enable Disable
SysLim1Latch	Latch system limit 1 fault	Latch Not Latch
SysLim1Type	System limit 1 check type (= or =)	= =
SysLimit1	Select alarm level in frequency Hz	0 to 100
SysLim2Enabl	Select system limit 2 (as above)	Enable Disable
SysLim2Latch	Latch system limit 1 fault	Latch Not Latch

Shunt V Tab (continued)

YTUR Shaft Voltage Monitor	Description	Select Option ✓ or Enter Value
SysLim2Type	System limit 1 check type (= or =)	= =
SysLimit2	Select alarm level in frequency Hz	0 to 100
TMR_DiffLimit	Diag Limit, TMR input vote difference, in engineering units	0 to 100

Shunt C Tab

YTUR Shaft Current Monitor	Description	Select Option ✓ or Enter Value
ShuntOhms	Shunt ohms	0 to 100
ShuntLimit	Shunt maximum test ohms	0 to 100
BrushLimit	Shaft (Brush) maximum ohms	0 to 100
SysLim1Enabl	Select system limit 1	Enable Disable
SysLim1Latch	Select whether alarm will latch	Latch Not Latch
SysLim1Type	Select type of alarm initiation	= =
SysLimit1	Current Amps, select alarm level in Amps	0 to 100
SysLim2Enabl	Select system limit 2	Enable Disable
SysLim2Latch	Select whether alarm will latch	Latch Not Latch
SysLim2Type	Select type of alarm initiation	= =
SysLimit2	Current Amps, select alarm level in Amps	0 to 100
TMR_DiffLimit	Diag Limit, TMR input vote difference, in engineering units	0 to 100

PT Tab (Gen and Bus)

YTUR Potential Transformer	Description	Select Option ✓ or Enter Value
PT_Input	PT primary in engineering units (kv or percent) for PT_Output	0 to 1,000
PT_Output	PT output in volts rms, for PT_Input – typically 115	0 to 150
SysLim1Enabl	Select system limit 1	Enable Disable
SysLim1Latch	Select whether alarm will latch	Latch Not Latch
SysLim1Type	Select type of alarm initiation	= =
SysLimit1	Current Amps, select alarm level in Amps	0 to 1000

PT Tab (Gen and Bus) (continued)

YTUR Potential Transformer	Description	Select Option ✓ or Enter Value
SysLim2Enabl	Select system limit 2	Enable Disable
SysLim2Latch	Select whether alarm will latch	Latch Not Latch
SysLim2Type	Select type of alarm initiation	= =
SysLimit2	Current Amps, select alarm level in Amps	0 to 1000
TMR_DiffLimit	Diag Limit, TMR input vote difference, in engineering units	0 to 1000

Circuit Breaker Tab

YTUR Circuit Breaker	Description	Select Option ✓ or Enter Value
SystemFreq	Select frequency in Hz	60 50
CB1CloseTime	Breaker 1 closing time, ms	0 to 500
CB1AdaptLimt	Breaker 1 self adaptive limit, ms	0 to 500
CB1AdaptEnab	Enable breaker 1 self adaptive adjustment	Enable Disable
CB1FreqDiff	Breaker 1 special window frequency difference, Hz	0.15 to 0.66
CB1PhaseDiff	Breaker 1 special window phase Diff, degrees	0 to 20
CB1DiagVoteEnab	Enable voting disagreement diagnostic	Enable Disable
CB2CloseTime	Breaker 2 closing time, ms (as above)	0 to 500
CB2 AdaptLimit	Breaker 2 self adaptive limit, ms	0 to 500
CB2 AdaptEnabl	Enable breaker 2 self adaptive adjustment	Enable Disable
CB2FreqDiff	Breaker 2 special window frequency difference, Hz	0.15 to 0.66
CB2PhaseDiff	Breaker 2 special window phase diff, degrees	0 to 20
CB2DiagVoteEnab	Enable voting disagreement diagnostic	Enable Disable

Relays Tab

YTUR Relays	Description	Select Option ✓ or Enter Value
PTR_Output	Primary protection relay used/unused	Unused Used
DiagVoteEnab	Enable voting disagreement diagnostic	Enable Disable

E-Stop Tab

YTUR E-Stop	Description	Select Option ✓ or Enter Value
DiagVoteEnab	Enable voting disagreement diagnostic	Enable Disable

TTUR Jumper

Jumper	Select ✓
JP1	TMR SMX
JP2	TMR SMX

TRPA (P1 and P2 jumpers)

Speed Input Connections	Function	Jumper
Wire to all 12 pulse inputs:	Each set of four pulse inputs goes to its own dedicated YTUR I/O pack.	Cannot use jumper.
PR1_R – PR4_T		Place in STORE position.
Wire to TTL pulse inputs:	Each set of two pulse inputs goes to its own dedicated YTUR I/O pack.	Cannot use jumper.
TTL1_R – TTL2_T		Place in STORE position.
Wire to bottom 4 pulse inputs only: PR1_R – PR4_R	The same set of signals is fanned to all the YTUR I/O packs.	Use jumper.
NO wiring to TTL1_R-TTL2_T or PR1_S-PR4_T		Place over pin pairs.
Wire to bottom 2 pulse inputs:	Cannot fan the TTL signals. Only the R YTUR will receive data.	Cannot use jumper.
TTL1_R – TTL2-R		Place in STORE position.

TRPA Jumper

Jumper	Select ✓
P1	FAN STORE
P2	FAN STORE

Notes

6 Proof Tests

Certain periodic proof tests must be satisfied to be eligible for IEC-61511 SIL certification. The testing schedule and resources are dependent on the designated proof test interval.

This test plan is to be used to validate SIL requirements for the Mark VIeS Safety Control during proof testing. Proof tests shall be conducted periodically to reveal any faults that may be undetected by system diagnostics during normal operation.

This test plan provides the following:

- Identifies the nature and extent of tests necessary to verify that the Mark VIeS Safety Control is fully compliant with SIL requirements
- Identifies equipment and describes test methodologies used to provide 99% proof test coverage

All test equipment must have up-to-date calibrations. Record the make, model, serial numbers, and calibration dates in the test record. The accuracy of measuring devices adds to the acceptance criteria.

Where possible, replace the terminal board field-wired terminal block with a test block to preserve field wiring with minimum disturbance.

These test procedures do not require configuration modifications to an existing SIS. Where system configurations are listed these are suggested configurations for test purposes. If the configuration does not match the system under test, either the test does not apply or the test results need to be adjusted.

Before each test, perform the following:

- Verify that no diagnostic alarms are present.
- Bypass any safety loop being tested or take other action to avoid an inadvertent trip.
- Check for inadvertent or unauthorized application changes by checking the *Branding Code* and compare with the application code recorded after commissioning or after the last authorized and verified change. Verify that the *Branding Code* matches the application code.

6.1 Proof Test Requirements

TMR and dual system configurations have automatic voting comparison diagnostics. This diagnostic provides random failure detection. The system and the voting diagnostics can be tested through the field device test procedure if field device test procedures include the following, and the alarm system has been checked to verify that no comparison diagnostics have been generated by the test.

For each safety loop when power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the comparison diagnostic should indicate a fault. When power that exceeds the hardware fault tolerance is removed from I/O packs, the system fails to its configured safe state, also for:

YAIC: Each analog sensor should be separately tested, one sensor at a time. Each test, if practicable, should range the sensor beyond the normal range of operation within the upper and lower limits of the sensors detectable range. Each output is tested when the output is ranged through a full range transition required to test the field device. When power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the system should maintain the required output.

YDIA: Each sensor should be tested causing a logical transition on the controller.

YDOA: Stimulate the safety function such that the output makes a transition. When power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the system should maintain the required output. Any output failures generate an error indication.

YHRA: Each analog sensor connected to an input should be tested separately. Each output is tested when the output is ranged through a full scale transition required to test the field device. The YHRA is a simplex only board, fault detection and failure modes are tested per the 61511 certified application code.

YTCC: Thermocouple inputs may be tested in place if an independent reference temperature is available to compare. Open TC detection can be tested by disconnecting one lead per TC at the terminal board screws. The cold junction temperature is tested by checking the temperature with the ToolboxST Cold Junction tab.

YVIB: Each sensor connected to an input should be separately tested, one sensor at a time (VibProx, VibProx-KPH, VibSiesmic, PosProx). Each test (if practicable) should range the sensor beyond the normal range of operation within the upper and lower limits of the sensors detectable range. Key Phasor***** input accuracy can be tested in place if a reference speed is available to compare. When power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the system should maintain the required output.

YPRO: Speed inputs are tested when input signals are varied and compared to the reference signal. E-Stop and contact input interlocks are tested when actuated and ETRs are observed to drop out. When power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the system should maintain the required output.

YSIL: A feature enhanced version of the YPRO that includes Speed Inputs, E-Stop, ETR's, provisions for contact inputs, relay outputs, thermocouple inputs, and flame detectors.

YTUR: Speed inputs are tested when input signals are varied and compared to the reference signal. Flame detector (Gieger-Muller) inputs are tested when presence of flame is observed. E-Stop input is tested when actuated and PTRs are observed to drop out. When power (or the communications cable) is removed from one I/O pack in a hardware fault tolerant channel, the system should maintain the required output.

6.1.1 Simplex Systems

Simplex systems do not benefit from having comparison diagnostics between the redundant controllers. Therefore, functional testing is the most effective way to detect random failures within the controller.

6.2 YAIC/YHRA Test Procedures

6.2.1 Input Accuracy

General:

- Test the accuracy of the YAIC or YHRA pack analog inputs for the configured I/O pack
- Test out of range detection for the configured I/O pack

Test Setup:

1. Obtain a multimeter and a signal source capable of generating current and voltages within the ranges of the configured YAIC pack.
2. Confirm configured limits for 4-20 mA input types. If configured for ranges other than 4-20 mA, adjust the test limits accordingly.

Note Channels 9 and 10 only allow current input; do not test input voltage on these channels.

A set of test values are provided in the following table. Use only those test values associated with the configured I/O point. Configuration changes are not required.

Test Details:

- For the configured I/O, select the appropriate test values from the following table and apply them to the input.
- Document the value that the YAIC reads for each test value, as seen in the *Input* tab in the ToolboxST application.
- Perform the above tests for each configured input channel.

Acceptance Criteria:

- All measured values must be within 2% of the full range input values for the input accuracy test to be accepted.
- For out of range values using the ToolboxST application, confirm that the YAIC alerts the system that the input is out of range through the *Diagnostics* tab and that the channel goes unhealthy.

Test Values for Configuration Settings

Configured Input Type	Test Values	Expected Reading
1 mA	-1.1 mA	Out of Range Diagnostic
1 mA	-1 mA	-1 mA ±.04
1 mA	-0.5 mA	-0.5 mA ±.04
1 mA	0.5 mA	0.5 mA ±.04
1 mA	1 mA	1.0 mA ±.04
1 mA	1.1 mA	Out of Range Diagnostic
↓	↓	↓
4-20 mA	3 mA	Out of Range Diagnostic
4-20 mA	4 mA	4 mA ±.4
4-20 mA	8 mA	8 mA ±.4
4-20 mA	12 mA	12 mA ±.4
4-20 mA	16 mA	16 mA ±.4
4-20 mA	20 mA	20 mA ±.4
4-20 mA	22 mA	Out of Range Diagnostic
↓	↓	↓
5 V	-6 V	Out of Range Diagnostic
5 V	-5 V	-5.0 V ±.2
5 V	-2.5 V	-2.5 V ±.2
5 V	0 V	0.0 V ±.2
5 V	2.5 V	2.5 V ±.2
5 V	5 V	5.0 V ±.2
5 V	6 V	Out of Range Diagnostic
↓	↓	↓
10 V	-12 V	Out of Range Diagnostic
10 V	-10 V	-10.0 V ±.4
10 V	-5 V	-5.0 V ±.4
10 V	0 V	0.0 V ±.4
10 V	5 V	5.0 V ±.4
10 V	10 V	10.0 V ±.4
10 V	12 V	Out of Range Diagnostic

6.2.2 Output Accuracy

General:

To test the accuracy of the YAIC pack analog outputs for the configured I/O packs.

Test Setup:

Connect a multimeter to the configured mA outputs.

Add a load to the output of approximately 250 Ω or meter in line with actual load device.

Test Details:

1. Connect the first channel of the output of the YAIC pack to a multimeter capable of measuring voltage and current.
2. Set the output of the pack to the first value in the following table. To set the output, go to the *Output* tab in the ToolboxST application and change the value of AnalogOutputxx.
3. Record the measured output current (mA) reading for this channel and output level.
4. Repeat steps 2 and 3 for each value in the following table.
5. Repeat steps 1-4 above for all channels configured for mA outputs.

Acceptance Criteria:

All measured values must be within 2% of the expected output values for the accuracy test to be accepted.

Output Ranges to Test

Output Value	Expected Value
0 mA	0 mA ±.4
4 mA	4 mA ±.4
8 mA	8 mA ±.4
12 mA	12 mA ±.4
16 mA	16 mA ±.4
20 mA	20 mA ±.4

6.2.3 YAIC Low Source Voltage

General:

The common source voltage for the analog input loop voltages for two-wire transmitters is monitored to detect low loop voltage and provide fault tolerance for this function when more than one I/O Processor is present.

Test Setup:

Connect a multimeter to any configured mA outputs of the YAIC as in the section *Output Accuracy*.

Test Details:

1. Disconnect the 28 V dc Low Source Voltage power supply connection from the pack (for a TMR terminal board disconnect the power supply from two packs).
2. Confirm that all the inputs go unhealthy and that the outputs drop to 0 mA.

Acceptance Criteria:

With the pack's power removed, the pack should turn the inputs unhealthy and drop any configured output channels to 0 mA current.

6.3 YDIA Test Procedures

Items that are configurable in the YDIA pack are identified in this test plan by including (CFG) at the end of the name of the item. Any configurable items that must be set for a particular test are defined in the detailed test instructions below. If a setting is not given for a configurable item, then it is not relevant to that test.

Unless otherwise noted in the test plan, the tester should verify that there are no diagnostics faults on the YDIA pack under test prior to performing each test case.

Any diagnostic fault(s) that are expected to occur as a result of performing a test case will be detailed in the acceptance criteria for the test case.

If additional diagnostics faults are generated in the course of testing that are not detailed in the acceptance criteria, they must be fully explained prior to acceptance of the test.

The following tests can be performed in any order. Individual steps within a test should be performed in the order presented.

6.3.1 Digital Input Status

General:

This tests the following items that are configurable on each digital input from the ToolboxST application and verifies that the controllers can receive the input data.

- ContactInput(CFG) (Used/Unused)
- SignalInvert(CFG) (Normal/Invert)
- DiagVoteEnab(CFG) (Enable/Disable)

Test Setup:

Perform the appropriate test case on each of the inputs as they are configured.

Test Detail:

Test Case 1: Test Input Used and Normal

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Normal
- DiagVoteEnab(CFG) = Enable

1. Verify that with the input open, all three controllers indicate the status of the input as *False*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)* and verify that each controller (R, S, T) correctly reads the status of the input as *True* and that there is no voting disagreement diagnostic.
3. Check that there is no cross-interference by verifying that the status of all other inputs is *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *True*, all inputs not jumpered have a status of *False*, and there are no voting diagnostics.

Test Case 2: Test Input Used and Invert

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Invert

1. Verify that with the input open, all three controllers indicate the status of the input as *True*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)*.
3. Verify that each controller (R, S, T) correctly reads the status of the input as *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *False*, all inputs not jumpered have a status of *True*, and there are no voting diagnostics.

6.3.2 YDIA Low Source Voltage

General:

This is a functional test that verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out of limits, and performs an orderly shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Detail:

1. Disconnect the 28 V dc power supply connection from the pack, in a TMR system disconnect the power connection from two packs.
2. Confirm that all the inputs go unhealthy (for loss of power on one pack of TMR look for disagreement diagnostic).

Acceptance Criteria:

When the supply voltage is < 16 ±1 V dc, a diagnostic is generated, and all inputs go unhealthy.

6.4 YDOA Test Procedures

Items that are configurable in the YDOA pack are identified by including (CFG) at the end of the name of the item. Any configurable items that must be set for a particular test are defined in the detailed test instructions below. If a setting is not given for a configurable item, then it is not relevant to that test.

Unless otherwise noted in the test plan, the tester should verify that there are no diagnostics faults on the YDOA pack under test prior to performing each test case.

Any diagnostic fault(s) that are expected to occur as a result of performing a test case will be detailed in the acceptance criteria for the test case.

If additional diagnostics faults are generated in the course of testing that are not detailed in the acceptance criteria, they must be fully explained prior to acceptance of the test.

The following tests can be performed in any order. Individual steps within a test should be performed in the order presented.

6.4.1 Digital Output Control

General:

This is a functional test that verifies that the Mark VIeS controller can control each output, that outputs are controlled through fault tolerant voting in TMR system, and that there is no cross-interference between outputs.

Relay actuation can be detected several ways:

1. If the device controlled by the relay is safe to actuate it may be used to determine the relay output state.
2. With wetting voltage applied the voltage at relay terminal board may be read.
3. Remove any wetting voltage and read the relay contact path resistance.

For method two and three, removing the terminal board screw blocks and replacing them with test blocks is recommended. For method three, a voltage reading prior to the resistance reading is recommended for safety purposes.

Test Setup:

Perform the appropriate test based on configuration of each of the outputs.

Test Case 1: Test Output Used and Normal

For outputs configured with:

- RelayOutput(CFG) = Used
- SignalInvert(CFG) = Normal

1. All outputs should initially be turned off.
2. Turn on the relay output.
3. Verify that only the correct relay on the terminal board is energized.
4. Repeat for all configured relay outputs.

Acceptance Criteria:

With the output turned on in the controller, only the correct relay on the terminal board is energized.

Test Case 2: Test Output Used and Invert

For outputs configured with:

- RelayOutput(CFG) = Used
- SignalInvert(CFG) = Invert

1. All outputs should initially be turned on.
2. Turn off the output.
3. Verify that only the correct relay on the terminal board is energized.
4. Repeat for all configured relay outputs

Acceptance Criteria:

With the output turned off in the controller, only the correct relay on the terminal board is energized.

6.4.1.1 SRSA Digital Output Control

The SRSA uses the JF1 connector to supply 125 V dc or 24 V dc power across the Bank A positive power connections, PWRAx_P and the power negative connections, PWRAx_N where x is equal to 2, 3, 4, 5 and 6. Likewise, the JF2 connector supplies power to the Bank B positive power connections, PWRBy_P and the power negative connections, PWRBy_N where y is equal to 8, 9, 10, 11 and 12.

The user closes the normally open contacts (NOx) in Bank A by first closing the mechanical force-guided relay, K1 followed by the solid-state relay, Kx. Similarly, the normally open contacts (NOy) in Bank B are closed by commanding the K7 mechanical relay to close followed by the solid-state relay, Ky.

Test Case 1: Test Output Used and Normal

For outputs configured with:

- RelayOutput(CFG) = Used
- SignalInvert(CFG) = Normal

All outputs should initially be turned off. Turn on the mechanical relay, K1 for Bank A or K7 for Bank B relay outputs. Turn on the Bank A solid-state relay, Kx where x=2, 3, 4, 5 or 6. Or turn on the Bank B solid-state relay, Ky where y=8, 9, 10, 11 or 12. Verify that only the correct relay on the terminal board is energized. Repeat for all configured relay outputs.

Acceptance Criteria:

With the output turned on in the controller, only the correct relay on the terminal board is energized.

Test Case 2: Test Output Used and Invert

For outputs configured with:

- RelayOutput(CFG) = Used
- SignalInvert(CFG) = Invert

All outputs should initially be turned off. Turn on the mechanical relay, K1 for Bank A or K7 for Bank B relay outputs. Turn on Bank A's solid-state relay, Kx where x=2, 3, 4, 5 or 6. Or turn on Bank B's solid-state relay, Ky where y=8, 9, 10, 11 or 12. Verify that only the correct relay on the terminal board is energized. Repeat for all configured relay outputs.

Acceptance Criteria:

With the output turned on in the controller, only the correct relay on the terminal board is energized.

6.4.2 Energized to Trip Applications

6.4.2.1 Relay Diagnostics for TRLYS1D

General:

This test verifies that the I/O pack is able to read feedback signals from the output circuits, to verify that outputs are in the correct state, and to generate diagnostic messages if they are not.

Test Setup:

This test is to be performed on the TRLYS1D with the following configurations as detailed below:

Test Case 1: Solenoid integrity on TRLYS1D (24 V dc)

Perform the following on all configured outputs.

1. Using a YDOA/TRLYS1D combination, connect 24 V dc power to connector JF1 on the terminal board with configure outputs:
    - RelayOutput(CFG) = Used
    - SignalInvert(CFG) = Normal
2. Connect a 0-250 Ω potentiometer across the NO and SOL terminals for the input under test; set the wiper to the middle of travel. All outputs should initially be turned off.
3. Gradually decrease the potentiometer resistance until a diagnostic is generated indicating that there is a failure of the external solenoid.
4. Disconnect the potentiometer and measure the resistance.
5. Reset the wiper of the potentiometer to the middle of travel and reconnect it to the terminals for the output under test.
6. Gradually increase the potentiometer resistance until a diagnostic indicates an external solenoid failure.
7. Disconnect the potentiometer and measure the resistance.

Acceptance Criteria:

When the output is de-energized and the external resistance is below 7 Ω, a diagnostic indicates solenoid failure. When the output is de-energized and the external resistance is above 200 Ω, a diagnostic indicates solenoid failure.

Test Case 2: Solenoid integrity on TRLYS1D (125 V dc)

Perform the following on all configured outputs.

1. Connect 125 V dc power to connector JF1 on the terminal board with configure outputs:
   - RelayOutput(CFG) = Used
   - SignalInvert(CFG) = Normal
2. Connect a 0-5K Ω potentiometer across the NO and SOL terminals for the input under test; set the wiper to the middle of travel. All outputs should initially be turned off.
3. Gradually decrease the potentiometer resistance until a diagnostic indicates an external solenoid failure.
4. Disconnect the potentiometer and measure the resistance.
5. Reset the potentiometer wiper to the middle of travel and reconnect it to the terminals for the output under test.
6. Gradually increase the potentiometer resistance until a diagnostic indicates an external solenoid failure.
7. Disconnect the potentiometer and measure the resistance.

Acceptance Criteria:

When the output is de-energized and the external resistance is below 122 Ω, a diagnostic is generated to indicate solenoid failure. When the output is de-energized and the external resistance is above 3250 Ω, a diagnostic indicates solenoid failure.

6.4.3 Low Source Voltage

General:

This test verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out-of-limits, and performs an orderly shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Details:

1. Disconnect the 28 V dc power supply connection from the pack (for TMR disconnect 28 V dc power supply connections to two packs).
2. Confirm that all the outputs are in their safe state, display unhealthy, and a diagnostic is generated.

Acceptance Criteria:

When the supply voltage is < 16 ±1 V dc, a diagnostic is generated, and all outputs go to their fail-safe state and display unhealthy.

6.5 YTCC Test Procedures

For TBTC-mounted YTCCs, a terminal board test terminal block facilitates maintaining the field wiring while performing thermocouple tests. If a test terminal block cannot be used, remove each thermocouple (TC) connection for each TC test. Reconnect when finished.

6.5.1 TC Input Accuracy

When two or more thermocouples are in near proximity and are expected to measure the same ambient temperature, an alternative test is to record and compare the temperature profile as the thermocouples cool from operational temperature and converge to the same ambient temperature. This alternative test could take several hours for ambient temperature to stabilize.

General:

To test the accuracy of the YTCC pack for various thermocouple configurations.

Test Setup:

Obtain a mV signal source, capable of fractional mV signals.

Alternative:

Use a calibrated heat source or thermocouple test set.

Test Details:

1. For the configured thermocouple, select the applicable thermocouple type from one of the following tables, *Type E Thermocouples*, *Type J Thermocouples*, *Type K Thermocouples*, *Type S Thermocouples*, or *Type T Thermocouples*.
2. Read the Cold Junction temperature from the ToolboxST application Cold Junction tab.
3. Look up the equivalent mV reading for the cold junction temperature under the table heading Cold Junction Compensation. Some interpolation is required.
4. Select one of the mV values in the thermocouple table and inject a mV signal such that the sum of the cold junction mV values and the injected mV signal at the terminal board input equals one of the mV values in the mV column of the thermocouple table. The temperature reading for that thermocouple reading displayed in the ToolboxST application should be equal to the temperature in the table.
5. Repeat step 4 for a second mV value in the thermocouple table.

Example:

For a type E thermocouple with a cold junction reading of 76.9 °F (25°C):

1. In the table, *Type E Thermocouples*, for 76.9 °F (25°C) the cold junction mV compensation is 1.49 mV.
2. Select 10 mV as a thermocouple test value.
3. Inject a mV signal of (10.0 – 1.5) = 8.5 mV at the terminal board screws.
4. The thermocouple should read 307 ±5 °F (152.8 ± -15 °C).

Acceptance Criteria:

All measured temperature signals should be within ±5 °F (-15°C) of the expected temperature for the input accuracy test to be accepted.

Type E Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.7	-5	-138.64
20	-0.373	0	32
30	-0.047	5	176.41

Type E Thermocouples (continued)

Cold Junction Compensation		Thermocouple	
40	0.264	10	307.35
50	0.594	15	430.12
60	0.924	20	547.99
70	1.261	25	662.81
80	1.597	30	775.69
90	1.939	40	998.58
100	2.281	45	1109.91
110	2.629		
120	2.977		
130	3.331		
140	3.685		
150	4.044		
160	4.403		
170	4.767		
180	5.131		

Type J Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.609	-5	-164.31
20	-0.332	0	32
30	-0.055	5	203.13
40	0.226	10	366.73
50	0.509	15	528.85
60	0.791	20	691.7
70	1.078	25	854.67
80	1.364	30	1015.14
90	1.654	35	1169.89
100	1.943	40	1317
110	2.236	45	1458.27
120	2.528		
130	2.823		
140	3.117		
150	3.414		
160	3.71		
170	4.009		
180	4.308		

Type K Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.476	-5	-244.73
20	-0.26	0	32
30	-0.043	5	251.51
40	0.177	10	475.2
50	0.398	15	692.29
60	0.619	20	904.78
70	0.844	25	1116.01
80	1.068	30	1329.48
90	1.295	35	1548.14
100	1.521	40	1773.32
110	1.749	45	2006.35
120	1.977		
130	2.207		
140	2.436		
150	2.667		
160	2.897		
170	3.128		
180	3.359		

Type S Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.063	0	32
20	-0.034	5	1070
30	-0.006	10	1896.5
40	0.025	15	2646
50	0.056		
60	0.087		
70	0.12		
80	0.152		
90	0.187		
100	0.221		
110	0.256		
120	0.291		
130	0.328		
140	0.365		
150	0.403		
160	0.44		
170	0.479		
180	0.518		

Type T Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.464	-5	-267.72
20	-0.253	0	32
30	-0.042	5	239.45
40	0.174	10	415.92
50	0.393	15	576.28
60	0.611	20	726.55
70	0.835		
80	1.06		
90	1.289		
100	1.519		
110	1.753		
120	1.988		
130	2.228		
140	2.468		
150	2.713		
160	2.958		
170	3.209		
180	3.459		

6.5.2 Open Thermocouple Inputs Detection

General:

This test demonstrates that the YTCC can successfully recognize when a thermocouple input becomes an open circuit.

Test Setup:

Short each configured thermocouple input from the positive to the negative terminal.

Test Details:

1. From the ToolboxST application, confirm that each of the configured thermocouple channels temperature readings is approximately the same as the cold junction.
2. Remove the short on the first channel to create an open circuit.
3. From the Toolbox application, confirm that the pack generates a diagnostic due to the open circuit.
4. Return the channel to a shorted condition.
5. Repeat steps 2 through 4 for each configured channel.

Acceptance Criteria:

All channels properly generate a diagnostic when the circuit is opened.

6.5.3 TC Input Low Source Voltage

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Details:

1. Disconnect the 28 V dc power supply connection from the pack (for a TMR terminal board disconnect the power supply from two packs).
2. Confirm that all the inputs go unhealthy.

Acceptance Criteria:

With the pack's power removed, the pack should turn the inputs unhealthy. Variables: PS18V_YTCC and PS28V_YTCC display *False* and *Unhealthy.*

6.6 YVIB Test Procedures

This test plan is designed for a generic configuration as described in each test detail section. Due to the large number of possible configurations for each signal type, some adjustment is necessary in the expected results if the configuration is different from the generic type. It is not necessary to alter the configuration to conduct this test plan but results may vary based on configuration.

6.6.1 Vibration (VibProx, VibProx-KPH) Input Accuracy

General:

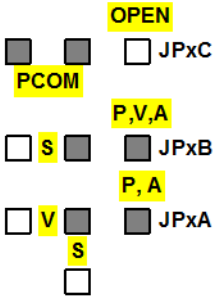
This test checks the accuracy of the YVIB vibration configured as VibProx, VibProx-KPH.

Test Setup:

Obtain a function generator capable of sinusoid signals of 10 V dc pp and ±5 V dc offsets.

To preserve field wiring, remove the wired terminal block and replace it with a test block for the following set of tests. Replace the field wired terminal block when testing is complete.

Test Details:



IS200TVBAS1A/S2A Vibration Terminal Board

Note Darkened box indicates proper jumper settings.

For each of the configure channels 1-8 configured for vibration inputs, the following generic configuration is assumed:

Configuration Parameters for All Channels											
Vib_PP_ Fltr	MaxVolt_ Prox	MinVolt_ Prox	MaxVolt_ KP	MinVolt_ KP	MaxVolt_ Seis	MinVolt_ Seis	MaxVolt_ Acc	MinVolt_ Acc	MaxVolt_ Vel	MinVolt_ Vel	SystemLimits
(0.04to 2.0 sec.)	(-4.0 to 0.0 Vdc)	(-24.0 to -16.0 Vdc)	(-4.0 to 0.0 Vdc)	(-24.0 to -16.0 Vdc)	(0.0 to 1.5 Vdc)	(-1.5 to 0.0 Vdc)	(-12.0 to 1.5 Vdc)	(-24.0 to -1.0 Vdc)	(-12.0 to 1.5 Vdc)	(-24.0 to -1.0 Vdc)	Enable Disable
0.1	-1.5	-18.5	-1.5	-22	1	-1	-8.5	-11.5	-8.375	-15.625	Enable

Gap (Gap 1-3) Configuration for GAP1_VIB1 thru GAP3_VIB3														
VIB_ Type4	Scale	Scale_Off	TMR_ DiffLimt	GnBiasOvride	Snsr_ Offset	Gain	LMlp cutoff	SysLim1 Enabl	SysLim1 Latch	SysLim1 Type	Sys Limit1	SysLim2 Enabl	SysLim2 Latch	SysLim2 Type	Sys Limit2
PosProx							1.5								
Unused							2.0								
VibLMAccel							2.5								
VibProx							3.0								
VibProx-KPH	volts/mil					1x	3.5								
VibSeismic	or	+/-13.3	(-1200 to	Disable	0 to x	2x	4.0								
VibVelomitor	volts/ips	Vdc	+1200)	Enable	Vdc	4x	4.5	Disable	Latch	<=	-1200 to	Disable	Latch	<=	-1200 to
VibProx-KPH	0.1	0	2	Enable	2.5	8x	5.0 Hz	Enable	NotLatch	>=	+1200	Enable	NotLatch	>=	+1200
						1x	5	Disable	n/a	n/a	n/a	Disable	n/a	n/a	n/a

Gap (Gap 4-8) Configuration for GAP4_VIB4 thru GAP8_VIB8														
VIB_ Type	Scale	Scale_ Off	TMR_ DiffLimt	GnBias Ovride	Snsr_ Offset	Gain	SysLim1 Enabl	SysLim1 Latch	SysLim1 Type	Sys Limit1	SysLim2 Enabl	SysLim2 Latch	SysLim2 Type	Sys Limit2
PosProx Unused VibProx VibProx-KPH VibSeismic VibVelomitor	volts/mil or volts/ips	+/-13.3 Vdc	(-1200 to +1200)	Disable Enable	+/-13.3 Vdc	1x 2x 4x 8x	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200
VibProx-KPH	0.1	0	2	Enable	2.5	1x	Disable	n/a	n/a	n/a	Disable	n/a	n/a	n/a

If the vibration inputs under test are configured differently from the settings listed above, the input signal or results should be adjusted to conform to the actual configuration. For example, if a high pass filter is employed, then the test signal frequency should be within the high pass frequency filter band.

In this test a 6 V dc pp with a –5 V dc offset will be read as a 60 mil vibration with a 50 mil gap.

Alternative:

Use a shaker table connected to vibration sensor to provide a reference input signal.

1. Configure the signal source to apply a 50 Hz sine wave (6 V dc pp) with a dc offset of –5 V dc.
2. Document the value that the YVIB reads for each value, as seen in I/O Live Value in the **Vib 1-8** tab. The first input channel will be called *VIB1*. The nominal value should be 60 mils.
3. Document the value that the YVIB reads for each value, as seen in I/O Live Value in the **Gap 1-3** tab. The first input channel will be called *GAP1_VIB1*. The nominal value should be 50.
4. Document the value that the YVIB reads for each value, as seen in I/O Live Value in the **Gap 4-8** tab. The first input channel will be called *GAP4_VIB4*. The nominal value should be 50.
5. Increase the signal frequency to 700 Hz.
6. Repeat steps 3, 4, and 5 for all vibration inputs configured as VibProx or VibProx-KPH.

Acceptance Criteria:

For Vibration signals (VIB1-8) 5-200 Hz 1% at 3 V dc pp (±0.03 V dc) or ±0.3 mils scaled to 0.1 V dc/mil.

For Vibration signals (VIB1-8) 200-700 Hz 5% at 3 V dc pp (±0.15 V dc) or ±1.5 mils scaled to 0.1 V dc/mil.

For Gap signal (GAP1_VIB1-GAP8_VIB8) 1% FS (±0.2 V dc) or ±2.0 mils scaled to 0.1 V dc/mil.

6.6.2 Vibration (VibSeismic) Input Accuracy

General:

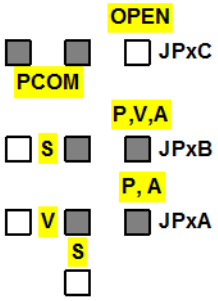
This test checks the accuracy of the YVIB vibration configured as VibSeismic inputs.

Test Setup:

Obtain a function generator capable of sinusoid signals of 10 V dc pp.

To preserve field wiring, remove the wired terminal block and replace it with a test block for the following set of tests. Replace the field wired terminal block when testing is complete.

Test Details:



IS200TVBAS1A/S2A Vibration Terminal Board

Gap (Gap 4-8) Configuration for GAP4_VIB4 thru GAP8_VIB8														
VIB_ Type	Scale	Scale_ Off	TMR_ DiffLimt	GnBias Ovride	Snsr_ Offset	Gain	SysLim1 Enabl	SysLim1 Latch	SysLim1 Type	Sys Limit1	SysLim2 Enabl	SysLim2 Latch	SysLim2 Type	Sys Limit2
PosProx Unused VibProx VibProx-KPH VibSeismic VibVelomitor	volts/mil or volts/ips	+/-13.3 Vdc	(-1200 to +1200)	Disable Enable	+/-13.3 Vdc	1x 2x 4x 8x	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200
VibSeismic	0.1	0	1200	Enable	0	1x	Enable	NotLatch	<=	32.5	Enable	NotLatch	>=	88

Note Darkened box indicates proper jumper settings.

If the Gap inputs under test are configured differently from the settings listed in the previous figure, the input signal or results should be adjusted to conform to the actual configuration. For example if the scale were configured to 0.2 V dc, then the live value would be ½ the expected value.

In this test, a 1.5 V dc pp with a 0 V dc offset will be read as a 7.5 mil vibration

1. Configure the signal source to apply a 50 Hz sine wave (1.5 V dc pp) with a 0 V dc offset.
2. Document the value that the YVIB reads as seen in I/O Live Value in the **Vib 1-8** tab. The nominal value should be 7.5 mils.
3. Repeat step 2 for all vibration inputs configured as VibSeismic.
4. Increase the signal frequency to 330 Hz.
5. Repeat step 2 for all vibration inputs configured as VibSeismic.

Acceptance Criteria:

Vibration seismic readings are accurate within 0.2 mils at 50 Hz and 0.5 mils at 660 Hz.

6.6.3 Position Proximeter (PosProx) Accuracy

This test checks the accuracy of the YVIB configured position proximeter inputs.

General Requirement Descriptions:

- The vibration input module provides 4 channels of signal conditioning for field wired position inputs.
- The analog input function can be configurable by the controller over IONet communications.

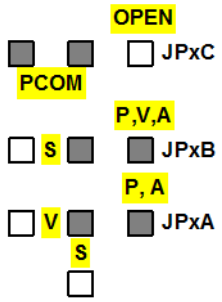
Test Setup:

Obtain a signal source capable of providing a dc signal of –1 to –9 V dc.

To preserve field wiring, remove the wired terminal block and replace it with a test block for the following set of tests. Replace the field wired terminal block when testing is complete.

Test Details:

This test is to be performed on the following terminal boards:



IS200TVBAS1A/S2A Vibration Terminal Board

Gap (Gap 9-12) Configuration for GAP9_POS1 thru GAP12_POS4														
VIB_ Type	**Scale**	**Scale_ Off**	**TMR_ DiffLimt**	**GnBias Ovride**	**Snsr_ Offset**	**Gain**	**SysLim1 Enabl**	**SysLim1 Latch**	**SysLim1 Type**	**Sys Limit1**	**SysLim2 Enabl**	**SysLim2 Latch**	**SysLim2 Type**	**Sys Limit2**
PosProx Unused	volts/mil or volts/ips	+/-13.3 Vdc	(-1200 to +1200)	Disable Enable	+/-13.3 Vdc	1x 4x	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200
PosProx	0.1	0	1200	Enable	2.5	1x	Enable	NotLatch	<=	32.5	Enable	NotLatch	>=	88

Note Darkened box indicates proper jumper settings.

If the Gap inputs under test are configured differently from the settings listed above, the input signal or results should be adjusted to conform to the actual configuration. For example if the scale were configured to 0.2 V dc then the live value would be ½ the expected value.

In this test a -1.75 V dc offset will be read as a 17.5 mil gap

1. For channels configured for PosProx.
2. Apply a -1.75 V dc signal to input channels 9 –12.
3. Document the value that the YVIB reads for each channel as seen in I/O Live Value in the **Gap 4-8** and **Gap 9-12** tabs. Nominal value is 17.5 mils.
4. Vary the displacement (gap) signal between -0.5 and -9.0 V dc. Gap readings should vary from 5 – 90 mils.

Acceptance Criteria:

All measured values must be within ±2.0 mils scaled 0.1 V dc.

Note The *Open Circuit Detection* test can be conducted simultaneously with this test for PosProx configured channels.

6.6.4 Keyphasor Transducer Accuracy

This test checks the accuracy of the YVIB position Keyphasor transducer input.

General:

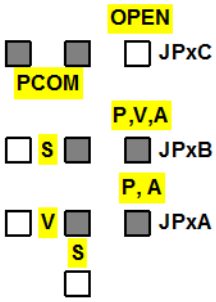
The vibration input module provides a channel for field wired Keyphasor transducer position input.

Test Setup:

To preserve field wiring, remove the wired terminal block and replace it with a test block for the following set of tests. Replace the field wired terminal block when testing is complete.

Test Details:

This test is to be performed on the following terminal boards:



IS200TVBAS1A/S2A Vibration Terminal Board

Note Darkened box indicates proper jumper settings.

Key Phasor (KPH) Configuration for GAP13_KPH1														
Scale_ Off	KPH_Thr shld	KPH_Typ e	TMR_Diff Limit	GnBiasO vride	Snsr_Offs et	Gain	SysLim1 Enabl	SysLim1 Latch	SysLim1 Type	Sys Limit1	SysLim2 Enabl	SysLim2 Latch	SysLim2 Type	Sys Limit2
+/-13.3 Vdc	1 to 5 Vdc	Slot Pedestal	(-1200 to +1200)	Disable Enable	+/-13.3 Vdc	1x 2x 4x 8x	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200	Disable Enable	Latch NotLatch	<= >=	-1200 to +1200
0	2	Slot	1200	Enable	5	1x	Enable	NotLatch	<=	20	Enable	NotLatch	>=	60

For YVIBS1A channel 13 or YVIBS1B channels 12 and 13 configured for Keyphasor transducer input:

1. Apply a 50 Hz pulse waveform with offset -5 V dc, 4 V dc pp, and a high side duty cycle > 55% to appropriate KeyPhasor channel(s).
2. If using YVIBS1A, document the value that the YVIBS1A reads for channel 13 from variable RPM_KPH1. Nominal value is 3000 rpm.
3. If using YVIBS1B, document the revolutions per minute YVIBS1B reads for channels 12 and 13 from the variables, RPM_KPH1 and RPM_KPH2. Nominal value is 3000 rpm.

Note A square wave has a 50% duty cycle and will not function.

Acceptance Criteria:

All measured values must be within ±20.0 rpm.

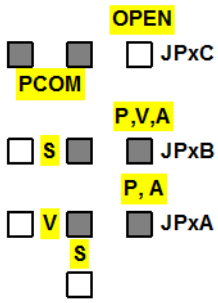
6.6.5 Open Circuit Detection

General:

Test the vibration input function open circuit detection for Proximity, Accelerometer and Velomitor sensor mode of operation.

Test Setup:

To preserve field wiring, remove the wired terminal block and replace it with a test block for the following set of tests. Replace the field wired terminal block when testing is complete.



IS200TVBAS1A/S2A Vibration Terminal Board

Note Darkened box indicates proper jumper settings.

Test Details:

Test Case 1: PosProx

1. For all inputs configured as position PosProx.
2. Apply a -5.0 V dc signal to the input.
3. Verify no diagnostic alarms for connected channels.
4. Open the input connection to all configured inputs.
5. Verify *Out of Limits or Saturated* and/or *Open Circuit* diagnostic alarm for all channels.

Test Case 2: VibLMAccel

1. For all inputs configured as VibLMAccel.
2. Apply a -9.0 V dc signal.
3. Verify no diagnostic alarms for connected channels.
4. Open the input connections to the VibLMAccel configured channels.
5. Verify *Out of Limits or Saturated* and/or *Open Circuit* diagnostic alarms for the channels.

Test Case 3: VibVelomitor

1. For all inputs configured as VibVelomitor.
2. Do not apply a test voltage to the inputs.
3. Open the input connection to the VibVelomitor channels.
4. Verify *Out of Limits or Saturated* and/or *Open Circuit* diagnostic alarm.

Acceptance Criteria:

Pack must be able to detect open circuit conditions and generate a diagnostic.

6.6.6 Low Source Voltage

General:

The common source voltage for the analog input loop voltages for two wire transmitters shall be monitored to detect low loop voltage and provide fault tolerance for this function when more than one I/O processor is present.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Details:

1. Disconnect the 28 V dc power supply connection from the pack (for a TMR terminal board disconnect the power supply from two packs).
2. Confirm that all the inputs go unhealthy.

Acceptance Criteria:

With the pack's power removed, the pack should turn the inputs unhealthy. PS28V_YVIB and PS18V_YVIB values goes to *False* and *Unhealthy.*

6.7 YPRO Test Procedures

Items that are configurable in the YPRO I/O pack are identified in this test plan by including (CFG) at the end of the name of the item. Any configurable items that must be set for a particular test are defined in the detailed test instructions below. If a setting is not given for a configurable item, it is not relevant to that test.

Unless otherwise noted in the test plan, the tester should verify that there are no diagnostics faults on the YPRO under test prior to performing each test case. Any diagnostic fault(s) expected to occur as a result of performing a test case are detailed in the acceptance criteria for the test case.

If additional diagnostics faults are generated in the course of testing that are not detailed in the acceptance criteria, they must be fully explained prior to acceptance of the test. The following tests can be performed in any order. Individual steps within a test should be performed in the order presented.

6.7.1 Contact Input Trip Tests

General:

This test verifies action of the contact input trips including trip logic in YPRO firmware.

Test Setup:

Select the Test Case below according to configuration of the Contact Inputs.

Test Detail:

These tests are relevant for TREG terminal boards.

Test Case 1: TripMode: Direct Trip (CFG)

1. **Energize Contact Input and reset trip relays**
   - **a.** Close contacts on E-stop button or connect a jumper across E-TRP (H) and TRP (L).
   - **b.** Clear all trip sources and reset the YPRO such that the emergency trip relays (ETR1-3) are picked up.
   - **c.** Verify that each controller (R, S, T) correctly reads the status of the contact input.

   Acceptance criteria:

   Controllers correctly read status of contact input.
2. **Initiate trip**
   - **a.** Open the contact input to generate a trip.
   - **b.** Verify that each controller (R, S, T) correctly reads the status of the contact input.

   Acceptance criteria:

   The controllers correctly read the status of the contact input and a diagnostic alarm message is generated indicating that the YPRO has tripped.
3. **Confirm trip cannot be reset**

Attempt to reset the trip by turning on the MasterReset output in the controller and confirm that the trip cannot be cleared with a reset as long as the contact remains open.

Acceptance criteria:.

The ETRs remain open and the diagnostic alarm message is generated indicating that the YPRO has tripped.

Test Case 2: TripMode: Conditional Trip (CFG)

1. **Test Conditional Trip – Negative**
   - **a.** Close contacts on E-stop button or connect a jumper to energize the contact input.
   - **b.** Clear all trip sources and reset the YPRO such that the emergency trip relays (ETR1-3) are picked up.

c. In the controller Vars-CI tab, set the value of trip#_inhibit to *True*.

d. Open E-stop button or remove the jumper from the contact input and confirm that the contact input does not cause a trip.

Acceptance criteria:

Contact input does not cause trip when inhibit signal is *True*.

2. Test Conditional Trip – Positive

a. Close contacts on E-stop button or connect a jumper to energize the contact input.

b. Clear all trip sources and reset the YPRO such that the emergency trip relays (ETR1-3) are picked up.

c. In the controller Vars-CI tab, set the value of trip#_inhibit to *False*.

d. Open E-stop button or remove the jumper from the contact input and confirm that the contact input does cause a trip.

Acceptance criteria:

Contact input causes trip when inhibit signal is *False*.

6.7.2 E-Stop Test

General:

This test verifies the E-stop trip logic in YPRO.

Test Setup:

These tests are relevant for TREG and TREA terminal boards.

Warning

These tests can move valves take precautions or use bypass procedures.

Test Case 1: E-stop on TREG terminal board

1. **Energize E-stop Input and reset trip relays**
   - **a.** Place E-stop button in run position.
   - **b.** Clear all trip sources and reset the YPRO such that the emergency trip relays (ETR1-3) are picked up.
   - **c.** Verify that each controller (R, S, T) correctly reads the status of the E-stop input (L5ESTOP1).

   Acceptance criteria:

   The trip relays reset to the running condition and all controllers correctly read status of contact input.
2. **Initiate trip**
   - **a.** Press the E-stop button.
   - **b.** Verify that each controller (R, S, T) correctly reads the status of the E-stop input (L5ESTOP1).

   Acceptance criteria:

   YPRO commands the trip relays to open all trip relay circuits, and the controllers correctly read the status of the E-stop input and a LED indication on the pack is generated indicating that the YPRO has tripped due to an E-stop.

Test Case 2: E-stop on TREA terminal board

1. **Energize E-stop Input and reset trip relays**

   a. Place E-stop button in run position.

   b. Clear all trip sources and reset the YPRO such that the emergency trip relays (ETR1-3) are picked up.

   c. Verify that each controller (R, S, T) correctly reads the status of the E-stop input (L5ESTOP1).

   Acceptance criteria:

   The trip relays reset to the running condition and all controllers correctly read status of L5ESTOP1_Fdbk = *True*, and all controllers read the status of L5ESTOP1 = *False*.

2. **Initiate trip**

   a. Press the E-stop button.

   b. Verify that each controller (R, S, T) correctly reads the status of the E-stop input (L5ESTOP1).

   Acceptance criteria:

   All three trip relays open with contact de-energization and the controllers correctly read the status of the contact input.

6.7.3 Speed Inputs Accuracy

General:

Simultaneously check characteristics of speed inputs (range, accuracy) and verifies that YPRO/SPRO/TREA support applications by allowing speed inputs to be sent to the controllers without cross-interference.

Alternative Accuracy Test:

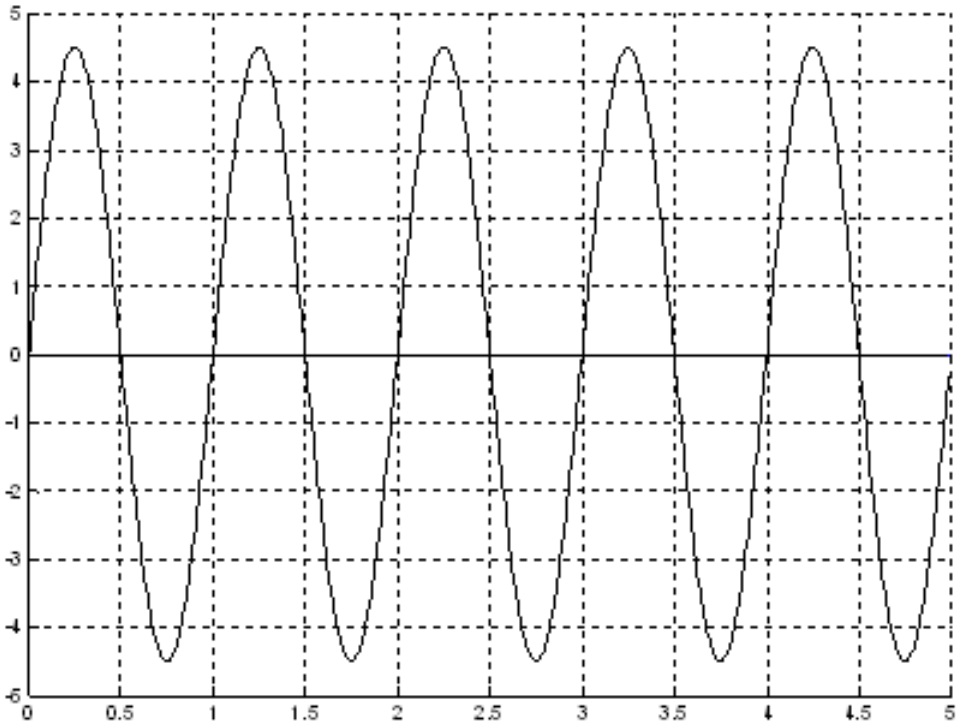
Compare YPRO speed signal at several different operating points with basic process control system (BPCS) speed signals.

Test Setup:

1. Connect an oscilloscope to the speed sensor terminal board inputs to measure the pulse rates from the speed pickups

Or

2. Disconnect the speed sensor inputs and configure a function generator for a 9 V dc pp sine wave output with zero offset to provide a reference speed signal to the pulse rate inputs.



Speed Input Accuracy

Perform the following on all configured pulse rate inputs. For at least 2 speeds in the range of 2 to 20,000 Hz, apply a speed signal and record the value of speed reported by the controller.

1. Verify that the channel being stimulated reads the correct value of speed and that all inputs that are not being stimulated read 0.
2. Repeat for each configured pulse rate inputs.

Acceptance Criteria:

The speed Input function will have < a 1% deviation between the actual steady state field signal and the reported value.

- Each channel reads the correct value of speed when stimulated.
- All inputs that are not being stimulated read zero.
- There should be no diagnostics.

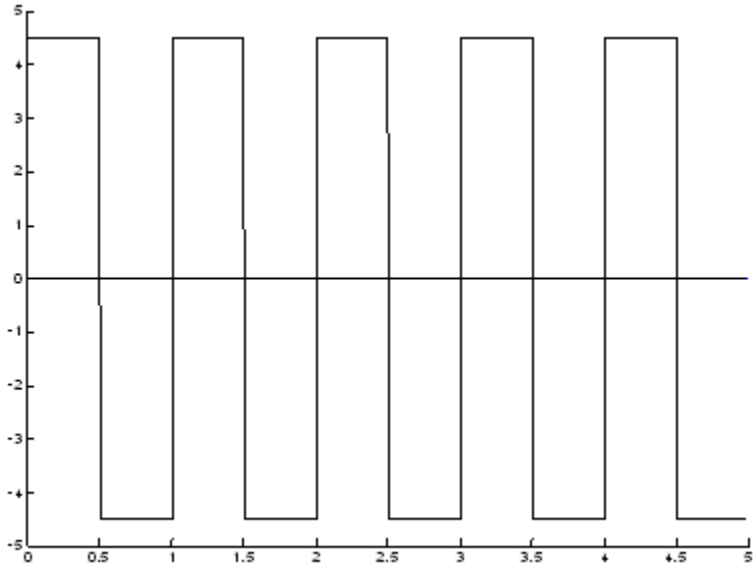
6.7.4 Overspeed Test

General:

The purpose of the overspeed test is to confirm an overspeed condition is properly detected and to exercise the emergency trip relays (ETR). Periodic testing that performs this function will meet the proof test requirements for this safety function. The following test procedure provides a method to perform this functional test.

Test Setup:

This test procedure uses one function generator output; FG1. For each test step, connect the function generator to the inputs indicated in the following figure. Configure the function generator output for square wave output, 9 V dc pp, 0 V dc offset.



Function Generator Inputs

Caution

Some function generators introduce large frequency deviations while incrementing in frequency, these deviations may cause an acceleration or deceleration trip if the I/O pack is configured for accl/decl trips.

Test Detail:

Unless otherwise noted, perform a MasterReset after each step that results in a trip.

Firmware Overspeed Trip OS_Setpoint

1. Connect FG1 to the first configured pulse rate input. Ramp the frequency of FG1 up until the YPRO trips. Record the signal on the pulse rate input and the status of the output contacts.
2. Attempt to reset the overspeed fault by sending a MasterReset from the controller.
3. Reduce frequency to below trip point and send a MasterReset.
4. Repeat for all configured pulse rate inputs.

Acceptance Criteria:

- The ETR contacts open when the frequency of FG1 reaches the value of OS_Setpoint(CFG), and a diagnostic is generated indicating that an overspeed trip occurred, and the controller input signal ComposTrip1 = *True.*
- Overspeed fault cannot be reset as long as the pulse rate signal is above the value of OS_Setpoint(CFG).

➢ **To perform the hardware overspeed trip on HWOS_Setpoint test**

1. Configure the firmware overspeed setpoint, OS_Setpoint(CFG) (*Pulse Rate* tab), to a speed greater than the hardware overspeed setpoint.
2. Download the firmware overspeed setpoint. An overspeed [ ] firmware setpoint configuration error diagnostic occurs, to clear the diagnostic set the OSn_Setpoint (*Vars-Speed* tab) to match the configuration value OS_Setpoint (*Pulse Rate* tab).
3. Connect FG1 to the first configured pulse rate input pair. Ramp the frequency of FG1 up until the PPRO trips. Record the signal on the pulse rate input and the status of the output contacts.
4. Attempt to reset the overspeed fault by sending a MasterReset from the controller.
5. Reduce frequency to significantly (at least 10%) below trip point and send a MasterReset.
6. Repeat for all configured pulse rate input pairs.
7. Restore the firmware, OS_Setpoint(CFG) (*Pulse Rate* tab), and signal space firmware overspeed setpoint, OSn_Setpoint (*Vars-Speed* tab), to their original value.

Acceptance Criteria:

- The ETR contacts open when the frequency of FG1 reaches the value of HWOS_Setpoint(CFG), and a diagnostic indicates that an overspeed trip occurred, and the controller input signal ComposTrip1 = *True*
- Overspeed fault cannot be reset as long as the pulse rate signal is above the value of HWOS_Setpoint(CFG).

6.7.5 Low Source Voltage

General:

This is a functional test that verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out of limits, and performs a shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Case:

1. Disconnect the 28 V dc power supply connection from the pack (for TMR disconnect two 28 V dc power supply connections).
2. Confirm that all the outputs are in their safe state, display unhealthy and a diagnostic is generated.

Acceptance Criteria:

When the supply voltage is < 16 V dc, a diagnostic is generated, all outputs go to their safe state and display unhealthy. Variables: PS18V_YPRO_/R/S/T and PS28V_YPRO_/R/S/T display *False* and *Unhealthy.*

6.8 YSIL Test Procedures

Items that are configurable in the YSIL I/O pack are identified in this test plan by including (CFG) at the end of the name of the item. Any configurable items that must be set for a particular test are defined in the detailed test instructions below. If a setting is not given for a configurable item, it is not relevant to that test.

Unless otherwise noted in the test plan, the tester should verify that there are no diagnostics faults on the YSIL under test prior to performing each test case. Any diagnostic fault(s) expected to occur as a result of performing a test case are detailed in the acceptance criteria for the test case.

If additional diagnostics faults are generated in the course of testing that are not detailed in the acceptance criteria, they must be fully explained prior to acceptance of the test. The following tests can be performed in any order. Individual steps within a test should be performed in the order presented.

6.8.1 E-Stop Test

General:

This test verifies the E-Stop trip logic in YSIL.

Test Setup:

These tests are relevant for TCSA terminal board.

Warning

These tests can move valves take precautions or use bypass procedures.

Test Case 1: E-Stop on TCSA terminal board

1. **Energize E-Stop Input and reset trip relays**
   - **a.** Place E-Stop button in run position.
   - **b.** Clear all trip sources and reset the YSIL such that the emergency trip relays (ETR1-3) are picked up. If configured as ETR, then ETR4–6 and ETR 7–9.
   - **c.** Verify that each controller (R, S, T) correctly reads the status of the E-Stop input (L5ESTOP1).

   Acceptance criteria:

   The trip relays reset to the running condition and all controllers correctly read status of contact input.
2. **Initiate trip**
   - **a.** Press the E-Stop button.
   - **b.** Verify that each controller (R, S, T) correctly reads the status of the E-Stop input (L5ESTOP1).

   Acceptance criteria:

   YSIL commands the trip relays to open all trip relay circuits, and the controllers correctly read the status of the E-Stop input and a LED indication on the pack is generated indicating that the YSIL has tripped due to an E-Stop.

6.8.2 Speed Inputs Accuracy

General:

Simultaneously check characteristics of speed inputs (range, accuracy) and verifies that YSIL/TCSA support applications by allowing speed inputs to be sent to the controllers without cross-interference.

Alternative Accuracy Test:

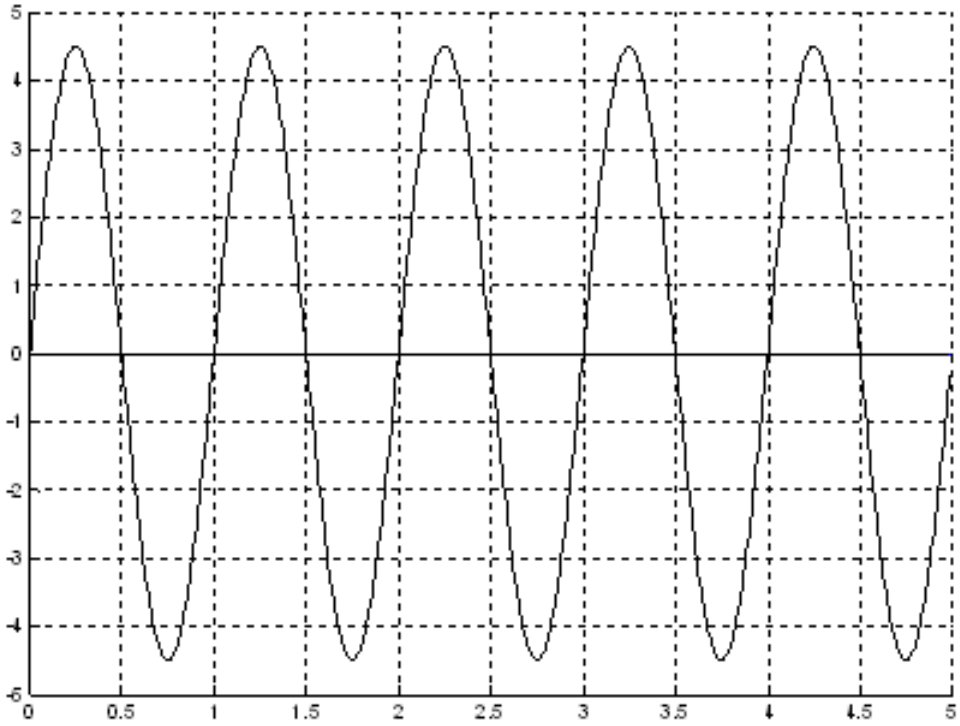
Compare YSIL speed signal at several different operating points with basic process control system (BPCS) speed signals.

Test Setup:

1. Connect an oscilloscope to the speed sensor terminal board inputs to measure the pulse rates from the speed pickups

Or

2. Disconnect the speed sensor inputs and configure a function generator for a 9 V dc pp sine wave output with zero offset to provide a reference speed signal to the pulse rate inputs.



Speed Input Accuracy

Perform the following on all configured pulse rate inputs. For at least 2 speeds in the range of 2 to 20,000 Hz, apply a speed signal and record the value of speed reported by the controller.

1. Verify that the channel being stimulated reads the correct value of speed and that all inputs that are not being stimulated read 0.
2. Repeat for each configured pulse rate inputs.

Acceptance Criteria:

The speed Input function will have < a 1% deviation between the actual steady state field signal and the reported value.

- Each channel reads the correct value of speed when stimulated.
- All inputs that are not being stimulated read zero.
- There should be no diagnostics.

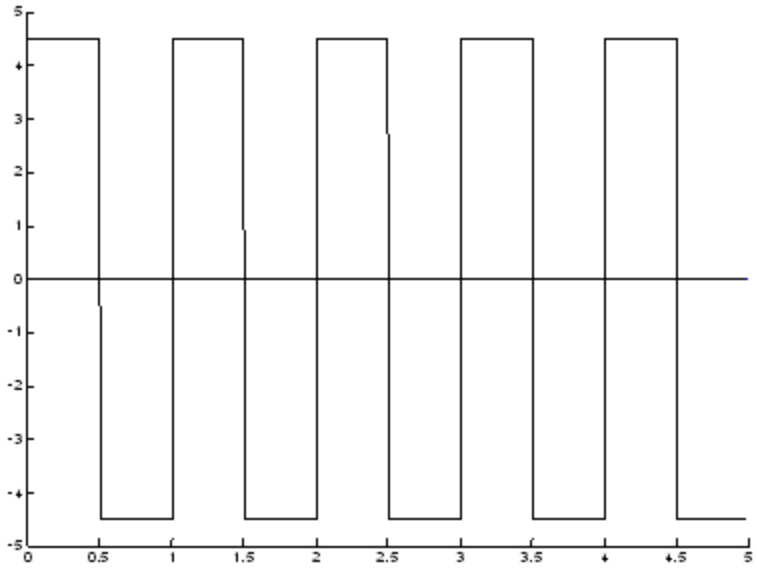
6.8.3 Overspeed Test

General:

The purpose of the overspeed test is to confirm an overspeed condition is properly detected and to exercise the emergency trip relays (ETR). Periodic testing that performs this function will meet the proof test requirements for this safety function. The following test procedure provides a method to perform this functional test.

Test Setup:

This test procedure uses one function generator output; FG1. For each test step, connect the function generator to the inputs indicated in the following figure. Configure the function generator output for square wave output, 9 V dc pp, 0 V dc offset.



Function Generator Inputs

Caution

Some function generators introduce large frequency deviations while incrementing in frequency, these deviations may cause an acceleration or deceleration trip if the I/O pack is configured for accl/decl trips.

Test Detail:

Unless otherwise noted, perform a MasterReset after each step that results in a trip.

Firmware Overspeed Trip OS_Setpoint

1. Connect FG1 to the first configured pulse rate input. Ramp the frequency of FG1 up until the YSIL trips. Record the signal on the pulse rate input and the status of the output contacts.
2. Attempt to reset the overspeed fault by sending a MasterReset from the controller.
3. Reduce frequency to below trip point and send a MasterReset.
4. Repeat for all configured pulse rate inputs.

Acceptance Criteria:

- The ETR contacts open when the frequency of FG1 reaches the value of OS_Setpoint(CFG), and a diagnostic is generated indicating that an overspeed trip occurred, and the controller input signal ComposTrip1 = *True.*
- Overspeed fault cannot be reset as long as the pulse rate signal is above the value of OS_Setpoint(CFG).

➢ **To perform the hardware overspeed trip on HWOS_Setpoint test**

1. Configure the firmware overspeed setpoint, OS_Setpoint(CFG) (*Pulse Rate* tab), to a speed greater than the hardware overspeed setpoint.
2. Download the firmware overspeed setpoint. An overspeed [ ] firmware setpoint configuration error diagnostic occurs, to clear the diagnostic set the OSn_Setpoint (*Vars-Speed* tab) to match the configuration value OS_Setpoint (*Pulse Rate* tab).
3. Connect FG1 to the first configured pulse rate input pair. Ramp the frequency of FG1 up until the YSIL trips. Record the signal on the pulse rate input and the status of the output contacts.
4. Attempt to reset the overspeed fault by sending a MasterReset from the controller.
5. Reduce frequency to significantly (at least 10%) below trip point and send a MasterReset.
6. Repeat for all configured pulse rate input pairs.
7. Restore the firmware, OS_Setpoint(CFG) (*Pulse Rate* tab), and signal space firmware overspeed setpoint, OSn_Setpoint (*Vars-Speed* tab), to their original value.

Acceptance Criteria:

- The ETR contacts open when the frequency of FG1 reaches the value of HWOS_Setpoint(CFG), and a diagnostic indicates that an overspeed trip occurred, and the controller input signal ComposTrip1 = *True*
- Overspeed fault cannot be reset as long as the pulse rate signal is above the value of HWOS_Setpoint(CFG).

6.8.4 Low Source Voltage

General:

This is a functional test that verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out of limits, and performs a shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Case:

1. Disconnect the 28 V dc power supply connection from the pack (for TMR disconnect two 28 V dc power supply connections).
2. Confirm that all the outputs are in their safe state, display unhealthy and a diagnostic is generated.

Acceptance Criteria:

When the supply voltage is < 16 V dc, a diagnostic is generated, all outputs go to their safe state and display unhealthy. Variables: PS18V_YSIL_/R/S/T and PS28V_YSIL_/R/S/T display *False* and *Unhealthy.*

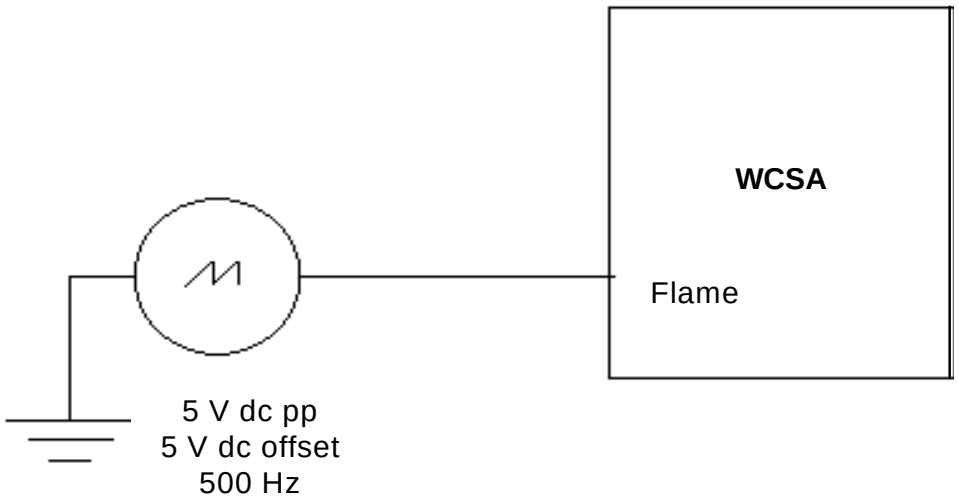
6.8.5 Flame Detection Inputs – Loss of Flame Detection

General:

This test checks for the YSIL to detect loss of flame and also verifies that no flame is the fail-safe state.

Test Setup:

For configured (Geiger-Muller) flame detector inputs; connect a function generator as indicated in the following figure:



Flame Detector Simulation

Test Detail:

Perform the following steps five times on each of the flame detector inputs:

1. Set the function generator to 500 Hz, 5 V dc pp saw tooth with a 5 V dc offset.
2. Verify that FDn_Flame = *True*.
3. Remove the function generator signal from the flame detector input.
4. Verify that FDn_Flame transitions to *False*.

Acceptance Criteria:

- FDn_Flame transitions to *False* when the function generator signal is disconnected.
- No diagnostics are generated during this test.

6.8.6 TCSA Analog Input Accuracy

General:

- Test the accuracy of the YSIL I/O pack analog inputs for the configured I/O pack

Test Setup:

1. Obtain a multimeter and a signal source capable of generating current and voltages within the ranges of the configured YSIL I/O pack.
2. Confirm configured limits for 4-20 mA input types.

A set of test values are provided in the following table. Use only those test values associated with the configured I/O point. Configuration changes are not required.

Test Details:

- For the configured I/O, select the appropriate test values from the following table and apply them to the input.
- Document the value that the YSIL reads for each test value, as seen in the *Input* tab in the ToolboxST application.
- Perform the above tests for each configured input channel.

Acceptance Criteria:

- All measured values must be within 2% of the full range input values for the input accuracy test to be accepted.
- For out of range values using the ToolboxST application, confirm that the YSIL alerts the system that the input is out of range through the *Diagnostics* tab and that the channel goes unhealthy.

Test Values for Configuration Settings

Configured Input Type	Test Values	Expected Reading
4-20 mA	3 mA	Out of Range Diagnostic
4-20 mA	4 mA	4 mA ±.4
4-20 mA	8 mA	8 mA ±.4
4-20 mA	12 mA	12 mA ±.4
4-20 mA	16 mA	16 mA ±.4
4-20 mA	20 mA	20 mA ±.4
4-20 mA	22 mA	Out of Range Diagnostic

6.8.7 SCSA Analog Input Accuracy

General:

- Test the accuracy of the YSIL I/O pack analog inputs for the configured I/O pack

Test Setup:

1. Obtain a multimeter and a signal source capable of generating current and voltages within the ranges of the configured YSIL I/O pack.
2. Confirm configured limits for 4-20 mA input types.

A set of test values are provided in the following table. Use only those test values associated with the configured I/O point. Configuration changes are not required.

Test Details:

- For the configured I/O, select the appropriate test values from the following table and apply them to the input.
- Document the value that the YSIL reads for each test value, as seen in the *Input* tab in the ToolboxST application.
- Perform the above tests for each configured input channel.

Acceptance Criteria:

- All measured values must be within 2% of the full range input values for the input accuracy test to be accepted.
- For out of range values using the ToolboxST application, confirm that the YSIL alerts the system that the input is out of range through the *Diagnostics* tab and that the channel goes unhealthy.

Test Values for Configuration Settings

Configured Input Type	Test Values	Expected Reading
4-20 mA	3 mA	Out of Range Diagnostic
4-20 mA	4 mA	4 mA ±.4
4-20 mA	8 mA	8 mA ±.4
4-20 mA	12 mA	12 mA ±.4
4-20 mA	16 mA	16 mA ±.4
4-20 mA	20 mA	20 mA ±.4
4-20 mA	22 mA	Out of Range Diagnostic

6.8.8 SCSA Composite Analog Trip Test

The YSIL can use any of the 4-20 mA analog inputs on the SCSA (AnalogInput01_R,S or T through AnalogInput16_R,S or T TMR input sets) in the Emergency Trip Relay (ETR) logic string. The user must configure AnalogInputx_R, S and T separately in the ToolboxST application to properly enable the analog input to function as a trip input for the ETRs. The user enables the SCSA analog input for tripping by doing the following for AnalogInputx_R, AnalogInputx_S and AnalogInputx_T:

1. Set the TripEnab(CFG) = Enable.
2. Set the TripSetPoint(CFG) = trip value (if exceeded will cause the ETRs to trip).
3. Set the TripDelay(CFG) = duration of time for analog input to exceed the TripSetPoint(CFG) before the trip request to ETRs will go True.

Note If the analog input falls below the TripSetPoint(CFG) for anytime during the TripDelay(CFG) time, the trip delay counter will be reset and the delay time starts over.

Test Case 1: Analog Input level below ETR Trip level

Test Setup:

1. Obtain a multi-meter and a signal source capable of generating current and voltages within the ranges of the configured YSIL I/O pack.
2. Confirm configured limits for 4-20 mA input types.
3. Configure TripEnab(CFG), TripSetPoint(CFG) and TripDelay(CFG) for AnalogInputx_R, S and T to trip at a level of 10 mA after a delay of 100 ms.

Test Details:

- Select an input value equal to 2% of full scale (0.4mA) below the TripSetPoint(CFG) value.
- Perform the above tests for each configured input channel.

Acceptance Criteria:

OPT LED must be green indicating an ETR trip has not occurred due to a Composite Analog Trip.

Test Case 2: Analog Input level above ETR Trip level

Test Setup:

1. Obtain a multi-meter and a signal source capable of generating current and voltages within the ranges of the configured YSIL I/O pack.
2. Confirm configured limits for 4-20 mA input types.
3. Configure TripEnab(CFG), TripSetPoint(CFG) and TripDelay(CFG) for AnalogInputx_R, S and T to trip at a level of 10 mA after a delay of 100 ms.

Test Details:

- Select an input value equal to 2% of full scale (0.4mA) above the TripSetPoint(CFG) value.
- Perform the above tests for each configured input channel.
- After removal of signal from analog channel under test, apply a master reset to clear the YSIL's ETR trip.

Acceptance Criteria:

OPT LED must be RED indicating an ETR trip has occurred due to a Composite Analog Trip.

6.8.9 Thermocouple Input Accuracy

When two or more thermocouples are in near proximity and are expected to measure the same ambient temperature, an alternative test is to record and compare the temperature profile as the thermocouples cool from operational temperature and converge to the same ambient temperature. This alternative test could take several hours for ambient temperature to stabilize.

General:

To test the accuracy of the YSIL pack for various thermocouple configurations.

Test Setup:

Obtain a mV signal source, capable of fractional mV signals.

Alternative:

Use a calibrated heat source or thermocouple test set.

Test Details:

1. For the configured thermocouple, select the applicable thermocouple type from one of the following tables, *Type E Thermocouples*, *Type J Thermocouples*, *Type K Thermocouples*, *Type S Thermocouples*, or *Type T Thermocouples*.
2. Read the Cold Junction temperature from the ToolboxST application Cold Junction tab.
3. Look up the equivalent mV reading for the cold junction temperature under the table heading Cold Junction Compensation. Some interpolation is required.
4. Select one of the mV values in the thermocouple table and inject a mV signal such that the sum of the cold junction mV values and the injected mV signal at the terminal board input equals one of the mV values in the mV column of the thermocouple table. The temperature reading for that thermocouple reading displayed in the ToolboxST application should be equal to the temperature in the table.
5. Repeat step 4 for a second mV value in the thermocouple table.

Example:

For a type E thermocouple with a cold junction reading of 76.9 °F (25°C):

1. In the table, *Type E Thermocouples*, for 76.9 °F (25°C) the cold junction mV compensation is 1.49 mV.
2. Select 10 mV as a thermocouple test value.
3. Inject a mV signal of (10.0 – 1.5) = 8.5 mV at the terminal board screws.
4. The thermocouple should read 307 ±5 °F (152.8 ± -15 °C).

Acceptance Criteria:

All measured temperature signals should be within ±5 °F (-15°C) of the expected temperature for the input accuracy test to be accepted.

Type E Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.7	-5	-138.64
20	-0.373	0	32
30	-0.047	5	176.41
40	0.264	10	307.35
50	0.594	15	430.12
60	0.924	20	547.99
70	1.261	25	662.81
80	1.597	30	775.69

Type E Thermocouples (continued)

Cold Junction Compensation		Thermocouple	
90	1.939	40	998.58
100	2.281	45	1109.91
110	2.629		
120	2.977		
130	3.331		
140	3.685		
150	4.044		
160	4.403		
170	4.767		
180	5.131		

Type J Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.609	-5	-164.31
20	-0.332	0	32
30	-0.055	5	203.13
40	0.226	10	366.73
50	0.509	15	528.85
60	0.791	20	691.7
70	1.078	25	854.67
80	1.364	30	1015.14
90	1.654	35	1169.89
100	1.943	40	1317
110	2.236	45	1458.27
120	2.528		
130	2.823		
140	3.117		
150	3.414		
160	3.71		
170	4.009		
180	4.308		

Type K Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.476	-5	-244.73
20	-0.26	0	32
30	-0.043	5	251.51
40	0.177	10	475.2
50	0.398	15	692.29
60	0.619	20	904.78

Type K Thermocouples (continued)

Cold Junction Compensation		Thermocouple	
70	0.844	25	1116.01
80	1.068	30	1329.48
90	1.295	35	1548.14
100	1.521	40	1773.32
110	1.749	45	2006.35
120	1.977		
130	2.207		
140	2.436		
150	2.667		
160	2.897		
170	3.128		
180	3.359		

Type S Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.063	0	32
20	-0.034	5	1070
30	-0.006	10	1896.5
40	0.025	15	2646
50	0.056		
60	0.087		
70	0.12		
80	0.152		
90	0.187		
100	0.221		
110	0.256		
120	0.291		
130	0.328		
140	0.365		
150	0.403		
160	0.44		
170	0.479		
180	0.518		

Type T Thermocouples

Cold Junction Compensation		Thermocouple	
Degrees F	**mV**	**mV**	**Degrees F**
10	-0.464	-5	-267.72
20	-0.253	0	32
30	-0.042	5	239.45
40	0.174	10	415.92

Type T Thermocouples (continued)

Cold Junction Compensation		Thermocouple	
50	0.393	15	576.28
60	0.611	20	726.55
70	0.835		
80	1.06		
90	1.289		
100	1.519		
110	1.753		
120	1.988		
130	2.228		
140	2.468		
150	2.713		
160	2.958		
170	3.209		
180	3.459		

6.8.10 Open Thermocouple Inputs Detection

General:

This test demonstrates that the YSIL can successfully recognize when a thermocouple input becomes an open circuit.

Test Setup:

Short each configured thermocouple input from the positive to the negative terminal.

Test Details:

1. From the ToolboxST application, confirm that each of the configured thermocouple channels temperature readings is approximately the same as the cold junction.
2. Remove the short on the first channel to create an open circuit.
3. From the Toolbox application, confirm that the pack generates a diagnostic due to the open circuit.
4. Return the channel to a shorted condition.
5. Repeat steps 2 through 4 for each configured channel.

Acceptance Criteria:

All channels properly generate a diagnostic when the circuit is opened.

6.8.11 Thermocouple Input Low Source Voltage

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Details:

1. Disconnect the 28 V dc power supply connection from the pack (for a TMR terminal board disconnect the power supply from two packs).
2. Confirm that all the inputs go unhealthy.

Acceptance Criteria:

With the pack's power removed, the pack should turn the inputs unhealthy. Variables: PS18V_YTCC and PS28V_YTCC display *False* and *Unhealthy.*

6.8.12 Digital Output Control

General:

This is a functional test that verifies that the Mark VIeS controller can control each output, that outputs are controlled through fault tolerant voting in TMR system, and that there is no cross-interference between outputs.

Relay actuation can be detected several ways:

1. If the device controlled by the relay is safe to actuate it may be used to determine the relay output state.
2. With wetting voltage applied the voltage at relay terminal board may be read.
3. Remove any wetting voltage and read the relay contact path resistance.

For method two and three, removing the terminal board screw blocks and replacing them with test blocks is recommended. For method three, a voltage reading prior to the resistance reading is recommended for safety purposes.

Test Setup:

Perform the appropriate test based on configuration of each of the outputs.

Test Case 1: Test Output Used and Normal

For outputs configured with:

- RelayOutput(CFG) = Used

1. All outputs should initially be turned off.
2. Turn on the relay output.
3. Verify that only the correct relay on the terminal board is energized.
4. Repeat for all configured relay outputs.

Acceptance Criteria:

With the output turned on in the controller, only the correct relay on the terminal board is energized.

6.8.13 Contact Input Low Source Voltage

General:

This is a functional test that verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out of limits, and performs an orderly shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Detail:

1. Disconnect the 28 V dc power supply connection from the pack, in a TMR system disconnect the power connection from two packs.
2. Confirm that all the inputs go unhealthy (for loss of power on one pack of TMR look for disagreement diagnostic).

Acceptance Criteria:

When the supply voltage is < 16 ±1 V dc, a diagnostic is generated, and all inputs go unhealthy.

6.8.14 SCSA Contact Input Status

General:

This tests the following items that are configurable on each digital input from the ToolboxST application and verifies that the controllers can receive the input data.

- ContactInput(CFG) (Used/Unused)
- SignalInvert(CFG) (Normal/Invert)
- DiagVoteEnab(CFG) (Enable/Disable)

Test Setup:

Perform the appropriate test case on each of the inputs as they are configured.

Test Detail:

Test Case 1: Test Input Used and Normal

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Normal
- DiagVoteEnab(CFG) = Enable

1. Verify that with the input open, all three controllers indicate the status of the input as *False*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)* and verify that each controller (R, S, T) correctly reads the status of the input as *True* and that there is no voting disagreement diagnostic.
3. Check that there is no cross-interference by verifying that the status of all other inputs is *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *True*, all inputs not jumpered have a status of *False*, and there are no voting diagnostics.

Test Case 2: Test Input Used and Invert

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Invert

1. Verify that with the input open, all three controllers indicate the status of the input as *True*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)*.
3. Verify that each controller (R, S, T) correctly reads the status of the input as *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *False*, all inputs not jumpered have a status of *True*, and there are no voting diagnostics.

6.8.15 TCSA Contact Input Status

General:

This tests the following items that are configurable on each digital input from the ToolboxST application and verifies that the controllers can receive the input data.

- ContactInput(CFG) (Used/Unused)
- SignalInvert(CFG) (Normal/Invert)

Test Setup:

Perform the appropriate test case on each of the inputs as they are configured.

Test Detail:

Test Case 1: Test Input Used and Normal

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Normal

1. Verify that with the input open, all three controllers indicate the status of the input as *False*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)* and verify that each controller (R, S, T) correctly reads the status of the input as *True* and that there is no voting disagreement diagnostic.
3. Check that there is no cross-interference by verifying that the status of all other inputs is *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *True*, all inputs not jumpered have a status of *False*, and there are no voting diagnostics.

Test Case 2: Test Input Used and Invert

All inputs that are configured with

- ContactInput(CFG) = Used
- SignalInvert(CFG) = Invert

1. Verify that with the input open, all three controllers indicate the status of the input as *True*.
2. Connect a jumper between *Input X (Positive)* and *Input X (Return)*.
3. Verify that each controller (R, S, T) correctly reads the status of the input as *False*.

Acceptance Criteria:

When the inputs are jumpered, all three controllers indicate the status as *False*, all inputs not jumpered have a status of *True*, and there are no voting diagnostics.

6.8.16 TCSA Contact Input Trip Tests

General:

This test verifies action of the contact input trips including trip logic in YSIL firmware.

Test Setup:

Select the Test Case below according to configuration of the Contact Inputs.

Test Detail:

These tests are relevant for TCSA terminal boards.

Test Case 1: TripMode: Direct Trip (CFG)

1. **Energize Contact Input and reset trip relays**

   a. Close contacts on E-Stop button or connect a jumper across E-TRP (H) and TRP (L).

   b. Clear all trip sources and reset the YSIL such that the emergency trip relays (ETR1-3) are picked up. If configured as ETR, then ETR4–6 and ETR7–9.

   c. Verify that each controller (R, S, T) correctly reads the status of the contact input.

   Acceptance criteria:

   Controllers correctly read status of contact input.

2. **Initiate trip**

   a. Open the contact input to generate a trip.

   b. Verify that each controller (R, S, T) correctly reads the status of the contact input.

   Acceptance criteria:

   The controllers correctly read the status of the contact input and a diagnostic alarm message is generated indicating that the YSIL has tripped.

3. **Confirm trip cannot be reset**

Attempt to reset the trip by turning on the MasterReset output in the controller and confirm that the trip cannot be cleared with a reset as long as the contact remains open.

Acceptance criteria:.

The ETRs remain open and the diagnostic alarm message is generated indicating that the YSIL has tripped.

Test Case 2: TripMode: Conditional Trip (CFG)

1. **Test Conditional Trip – Negative**
   - **a.** Close contacts on E-Stop button or connect a jumper to energize the contact input.
   - **b.** Clear all trip sources and reset the YSIL such that the emergency trip relays (ETR1-3) are picked up.
   - **c.** In the controller Vars-CI tab, set the value of trip#_inhibit to *True*.
   - **d.** Open E-Stop button or remove the jumper from the contact input and confirm that the contact input does not cause a trip.

   Acceptance criteria:

   Contact input does not cause trip when inhibit signal is *True*.
2. **Test Conditional Trip – Positive**
   - **a.** Close contacts on E-Stop button or connect a jumper to energize the contact input.
   - **b.** Clear all trip sources and reset the YSIL such that the emergency trip relays (ETR1-3) are picked up.
   - **c.** In the controller Vars-CI tab, set the value of trip#_inhibit to *False*.
   - **d.** Open E-Stop button or remove the jumper from the contact input and confirm that the contact input does cause a trip.

   Acceptance criteria:

   Contact input causes trip when inhibit signal is *False*.

6.8.17 TCSA ETR#_Open Test

General: This test verifies the Vars-Relay output Booleans, ETR1_Open thru ETR9_Open control of the Emergency Trip Relays (ETRs).

Test Setup: These tests check the response of the ETRs on the TCSA terminal board.

Warning

These tests can move valves. Take precautions or use bypass procedures.

Test Case 1: ETRs closed for non-trip case

1. Configure K4 – K6 and K7 – K9 in TripMode
   - **a.** Set TripMode to Enable for both sets of relays.
2. Enable K1_Fdbk – K9_Fdbk for Sequence of Events and Diagnostics
   - **a.** Set SeqOfEvents equal to Enable.
   - **b.** Set DiagVoteEnab equal to Enable.
3. Set ETRs in “non-trip” state
   - **a.** Set all ETR#_Open output Booleans to False.
   - **b.** Clear all trip sources and reset the YSIL such that the emergency trip relays (ETR1-9) are picked up.
4. Verify that the relay feedbacks, K1_Fdbk thru K9_Fdbk display the ETRs energized.

Acceptance Criteria: The emergency trip relays are closed and all controllers read the status correctly.

Test Case 2: ETRs opened for trip case

1. Initiate ETR Trip Condition
   a. Set ETR1_Open output Boolean to True.
2. Verify that the relay feedback, K1_Fdbk displays the ETR1 de-energized or open (Trip state).
3. Verify that the controllers read the trip state for K1.
4. Repeat steps 1 through 3 for all nine relays.

Acceptance Criteria: The emergency trip relays are open and all controllers read the status correctly.

6.9 YTUR Test Procedures

Configurable items in the YTUR pack are identified in this test plan by including (CFG) at the end of the name of the item. Any configurable items that must be set for a particular test are defined in the detailed test instructions below. If a setting is not given for a configurable item, it is not relevant to that test.

- Unless otherwise noted, verify that there are no diagnostics faults on the YTUR pack under test prior to performing each test case.
- Any diagnostic fault(s) that are expected to occur as a result of performing a test case are detailed in the acceptance criteria for the test case.
- If additional diagnostics faults are generated that are not detailed in the acceptance criteria, they must be fully explained prior to acceptance of the test.

The following tests can be performed in any order. Individual steps within a test should be performed in the order presented.

6.9.1 Speed Inputs Accuracy

General:

This test checks characteristics of speed inputs (range and accuracy) and verifies that YTUR supports applications by allowing speed inputs to be sent to the controllers without cross-interference.

Alternative Accuracy Test:

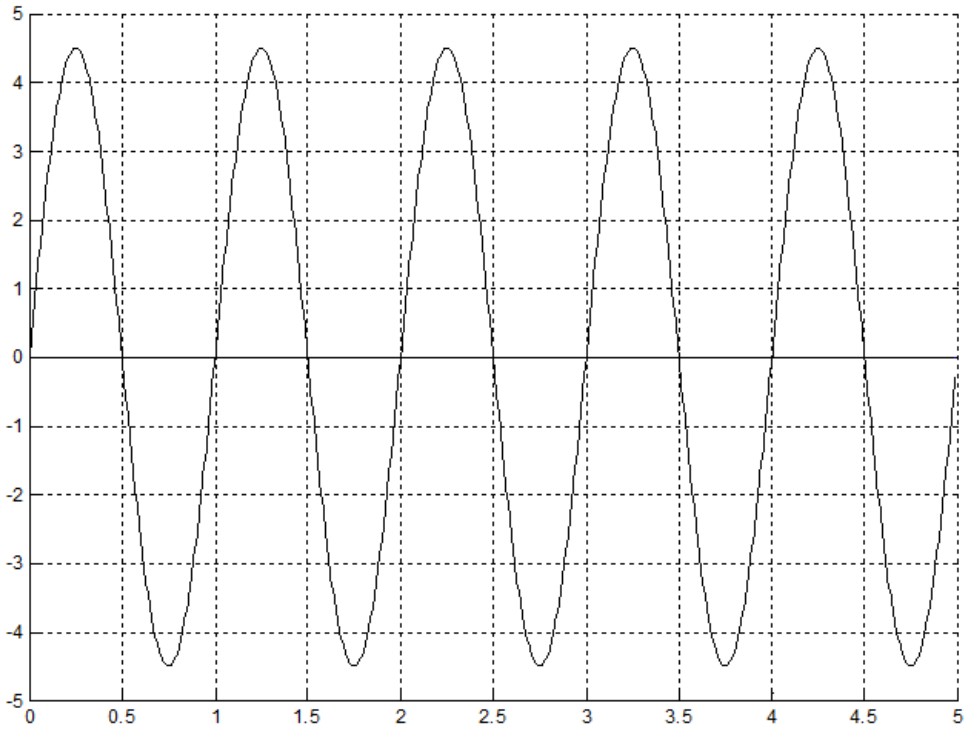
Compare YTUR speed signal at several different operating points with BPCS speed signals.

Test Setup:

Connect an oscilloscope to the speed sensor terminal board inputs to measure the pulse rates from the speed pickups

Or

Disconnect the speed sensor inputs and configure a function generator for a 9 V pp sine wave output with zero offset to provide a reference speed signal to the pulse rate inputs.



Speed Input Accuracy

Test Details

1. For at least two speeds in the range of 2 to 20,000 Hz, apply a speed signal and record the value of speed reported by the controller.
2. Verify that the channel being stimulated reads the correct value of speed and that all inputs which are not being stimulated read zero.
3. Repeat steps 1 and 2 on all configured pulse rate inputs.

Acceptance Criteria:

The speed Input function will have less than a 1% deviation between the actual steady state field signal and the reported value.

- Each channel reads the correct value of speed when stimulated.
- All inputs that are not being stimulated read zero.
- There should be no diagnostics.

6.9.2 TRPA E-Stop Input

General:

This test verifies that the E-Stop input, available on the TRPA, can drive the trip relay outputs and that this input can be used to cross-trip the YPRO trip logic.

Test Setup:

Note This test assumes that the trip solenoids are isolated from the circuit.

For each trip relay output, connect dummy loads to simulate trip solenoids as follows:

1. Connect one side of an appropriately sized resistor (10 kΩ 2 W) to the positive side of the trip relay output.
2. Connect the other side of the resistor to the positive side of a power supply (output voltage of power supply should be set to the nominal trip circuit voltage).
3. Connect the negative side of the power supply to the negative side of the trip relay output.

Test Details

1. Energize the E-Stop input and reset the trip relays (clear all trip sources and reset the YTUR such that the trip relays (PTR1-2) are picked up).
2. Verify that each controller (R, S, and T) correctly reads the status of the E-Stop input (KESTOP1_Fdbk).
3. Initiate an E-Stop Trip.
4. Verify the PTR's are de-energized (dropped out and that each controller (R, S, and T) correctly reads the status of the E-Stop input (KESTOP1_Fdbk).

Acceptance criteria:

When the E-Stop is energized (closed) the Primary Trip Relays (PTR) are energized (picked up), when the E-Stop is open the PTR's are de-energized (dropped out).

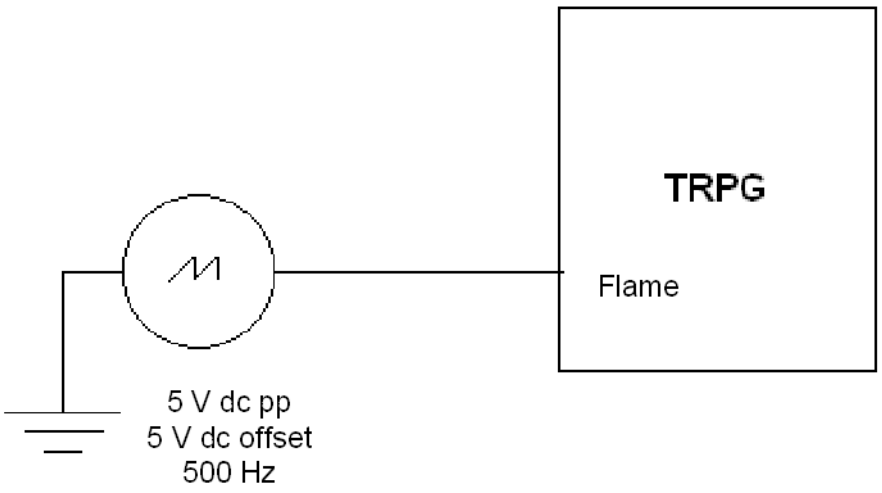
6.9.3 Flame Detection Inputs – Loss of Flame Detection

General:

This test checks for the YTUR to detect loss of flame and also verifies that no flame is the fail-safe state.

Test Setup:

For configured (Geiger-Muller) flame detector inputs; connect a function generator as indicated in the following figure:



Flame Detector Simulation

Test Detail:

Perform the following steps five times on each of the flame detector inputs:

1. Set the function generator to 500 Hz, 5 V dc pp saw tooth with a 5 V dc offset.
2. Verify that FDn_Flame = *True*.
3. Remove the function generator signal from the flame detector input.
4. Verify that FDn_Flame transitions to *False*.

Acceptance Criteria:

- FDn_Flame transitions to *False* when the function generator signal is disconnected.
- No diagnostics are generated during this test.

6.9.4 Low Source Voltage

General:

This test verifies that the pack monitors its 28 V dc supply, generates diagnostics if the supply is out of limits, and performs an orderly shutdown if power supply voltage is too low for safe operation.

Test Setup:

Prepare system for a fail-safe response from the I/O pack.

Test Case:

1. Disconnect the 28 V dc power supply connection from the pack (for TMR disconnect two 28 V dc power supply connections).
2. Confirm that all the outputs are in their safe state, display unhealthy and a diagnostic is generated.

Acceptance Criteria:

When the supply voltage is less than 16 ±1 V dc, a diagnostic is generated, all outputs go to their fail safe state and display unhealthy. Variables: PS18V_YTUR and PS28V_YTUR display *False* and *Unhealthy.*

Notes

Appendix: Determine Frame Input Client Completion Time

Use the following procedures to determine frame input completion time with Mark VIeS V06.00 (ControlST V07.02).

Note Information about the timing of frame input times is available in the Controller Advanced Diagnostics.

➢ **To view timing data**

1. Unlock the controller by selecting **Lock/Unlock** from the ToolboxST **Device** menu and clicking **Unlock**.
2. From the **View** menu, select **Diagnostics** and **Controller Advanced Diagnostics** to display the *Controller Advanced Diagnostics* dialog box.
3. Collect the timing information by selecting **Commands**, **Diagnostics**, **Sequencer**, **Client Data**, and then press **Send Command**.

Note Without resetting the timing data, the data will likely have overruns and invalid data as minimum and maximum times.

➢ **To determine maximum completion time**

1. From the *Controller Advanced Diagnostics* dialog box, reset the timing and overrun counters by selecting **Commands**, **Diagnostics**, **Sequencer**, and **Client Data Reset**, then press **Send Command**.
2. Wait for the controller to collect 100,000 samples. For example, if a 10 ms frame period is selected, wait for 100,000 / 100 samples per second / 60 seconds per minute = ~ 17 minutes.
3. View timing data. Refer to the procedure *To view timing data*.
4. Validate timing data. Refer to the procedure *To interpret timing data*.

➢ To interpret timing data

- The number of samples is the value in the Activation Count (*ActCount*) column (114206 shown in the following figure) and must be above 100,000 for a sufficiently large data set.
- The number of overruns (*OvrCount*) and re-overruns (*ReOvrCount*) must be 0.
- The maximum stop time of the three input clients, *ptp WhoISDc*, *egd Sweeper*, and the first *App* entry must be < 1.6 ms (1.600). These are highlighted in the following table as 1.489, 1.432 and 0.661, respectively.

Examples of Timing Data

Sequence Frame Clients († prefix indicates critical clients)

Note Use the -t option for client timing information.

Client	Start-Stop FrameStates	State	ActCount	OvrCount	ReOvrCount
ptp WhoIsDc	InputXfer -InputXfer	Armed	114206	0	0
† egd Sweeper	InputXfer -InputXfer	Armed	114206	0	0
† App	InputXfer -InputXfer	Armed	114206	0	0
† HP Blockware	App -App	Armed	114206	0	0
ptp Output	OutputXfer -OutputXfer	Armed TWait	114206	0	0
† App	OutputXfer -OutputXfer	Armed	114206	0	0
† App IONet	OutputXfer -OutputXfer	Armed TWait	114206	0	0

Sequence Frame Clients († prefix indicates critical clients)

Note Start and End times are offsets from start of frame.

Client	Start Time (ms)			Stop Time (ms)			Delta Time(ms)		
	Last	Min	Max	Last	Min	Max	Last	Min	Max
ptp WhoIsDc	1.400	1.281	1.446	1.442	1.324	1.489	0.042	0.039	0.070
† egd Sweeper	0.644	0.587	0.673	1.386	1.265	1.432	0.742	0.657	0.786
† App	0.033	0.026	0.049	0.620	0.575	0.661	0.587	0.546	0.629
† HP Blockware	1.461	1.343	1.507	2.215	2.085	2.251	0.754	0.727	0.785
ptp Output	7.300	7.251	7.370	7.387	7.336	8.037	0.087	0.067	0.745
† App	2.235	2.103	2.272	2.316	2.176	2.354	0.081	0.071	0.102
† App IONet	7.010	6.984	7.038	7.279	7.239	7.348	0.270	0.246	0.315
The highlighted values (Stop time Max data column) are the values that must be below 1.6 ms (1.600); individually not cumulatively.									

Examples of Application Timing

The following table lists a set of applications, configurations, and associated maximum input frame client completion time to use to determine if a given application will be compatible with the Mark VIeS Safety control. *This is for informational purposes only and is not meant to replace the user from collecting timing data from their actual physical system.*

Controller	# YSIL	# Generic TMR Yxxx	# YHRA	# Voted Booleans	Largest Max Stop Time (ms)
UCSBS1A	None	8 TMR (2 YAIC, 3 YDOA, 2 YDIA, 1 YTUR)	6 Simplex	924	1.22
	None	15 TMR (5 YAIC, 4 YDOA, 2 YDIA, 1 YTUR, 3 YVIB)	None	977	0.86
	1 TMR	15 TMR (4 YAIC, 3 YDOA, 5 YDIA, 3 YVIB)	4 Simplex	4000	1.49
UCSCS2A	1 TMR	23 TMR (3 YVIB, 6 YAIC, 7 TYDOA, 7 YDIA)	6 Simplex	31968 (max)	1.11